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RESEARCH ARTICLE

Experimental Validation of a Self - Timed Active Common - Mode Voltage Clamp in a 1 kW Interleaved Dual - Buck Transformer - less PV Inverter

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ABSTRACT: Removing the isolation transformer from a grid-connected photovoltaic (PV) inverter raises efficiency but leaves the parasitic capacitance of the array exposed to the common-mode voltage of the inverter. This paper reports the hardware validation of a 1 kW interleaved dual-buck full-bridge inverter with an active common-mode voltage clamp (IDBFB-ACMVC). Two 40 kHz buck legs interleaved by 180° shape a rectified sine, a 50 Hz insulated-gate bipolar transistor (IGBT) bridge unfolds it, and two anti-series MOSFETs with a 100 nF film capacitor join the buck output to the DC-link midpoint whenever neither buck switch is on. The clamp is switched by a NOR of the gate commands already generated for the two buck switches, so it uses no pulse-width modulation (PWM) channel of its own and carries no load current. The prototype was brought up in stages, from a perfboard unfolding bridge to a single printed circuit board with a dsPIC33 controller and gate drivers matched to the reference node and switching rate of each switch. From a 380 V DC bus, with a 100 nF capacitor emulating the array capacitance, the clamp reduces the measured leakage current from 46.4 mA to 9.6 mA RMS (79.3%), 3.1 times below the 30 mA threshold of VDE 0126-1-1. Efficiency peaks at 96.7% at 700 W and is 95.9% at 1 kW, voltage and current total harmonic distortion are 1.99% and 3.54%, and the power factor exceeds 0.99. Separating the measured leakage into its 100 Hz floor and its dead-time drift shows that the clamp removes about 81% of the drift.

Keywords: Active Clamp; Common-Mode Voltage; Dual-Buck Inverter; Hardware Prototype; Leakage Current; Photovoltaic Inverter; Transformerless Inverter; Unfolding Bridge.

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1. INTRODUCTION

Installed photovoltaic (PV) capacity passed 2.2 TW in 2024 [1]. The residential market has largely settled on transformerless inverters [2]. Removing the transformer is credited with an efficiency gain of 1 to 2% [3] and makes the inverter lighter, smaller and cheaper [4], but it also removes the galvanic barrier between the array and the grid. The cells and the earthed frame of every array form a parasitic capacitance, usually put at 50 to 150 nF per kWp for crystalline-silicon modules [5], and without the transformer any change in the inverter's common-mode voltage VCM drives a leakage current through it [6]. That current raises grid-current harmonics and losses, produces electromagnetic interference and creates a safety hazard [7]. Under VDE 0126-1-1 the inverter must disconnect within 0.3 s if the residual current jumps by 30 mA (faster for larger jumps) or if the continuous leakage passes 300 mA [3, 8]. IEC 62109-2 permits a 30 mA residual-current device (RCD) as the protective measure [9].

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Published topologies hold VCM constant in one of three ways [10]. H5, the Highly Efficient and Reliable Inverter Concept (HERIC) and H6 decouple the array from the grid while the bridge freewheels [11, 12]. Optimised H5 (oH5) and the H-bridge zero-voltage rectifier (HB-ZVR) clamp the freewheeling path at half the DC-link voltage [13, 14]. Neutral-point-clamped (NPC) circuits tie the grid neutral to the DC-link midpoint, which requires twice the DC-link voltage of a full bridge, and common-ground circuits tie the PV negative terminal to the grid neutral [15, 16]. Every one of these additions sits in the load-current path. In H5 and oH5 the grid current flows through three series switches while power is delivered [11, 17], the HERIC bypass pair and the NPC clamping devices conduct it during freewheeling [12, 18], and each such path adds conduction loss [11, 17]. The active clamps of oH5 and HB-ZVR take the inverse of a main-switch signal with a short delay added between the two [13, 14], so their gate timing has to be generated separately.

Dual-buck inverters remove the cause at the bridge leg instead. Each leg pairs one switch with one diode, so it has no shoot-through path and its high-frequency switch needs no dead-time [19, 20], and freewheeling takes place in dedicated diodes instead of MOSFET body diodes [21]. Interleaving two legs 180° apart reduces the output-current ripple and doubles its frequency [22], and an unfolding bridge switching only at line frequency restores the polarity at zero voltage and zero current [23]. Interleaved and single-inductor dual-buck full bridges keep VCM at either 0 or VPV for a whole half-cycle, which should in principle eliminate the leakage current [21, 24]. When these studies mention dead-time at all, it appears as a source of distortion at the zero crossing or as a shoot-through and reverse-recovery hazard [11, 21, 24]. Apart from junction-capacitance effects at mode transitions [19], what VCM does while neither buck switch conducts has not been analysed.

The interleaved dual-buck full-bridge inverter with an active common-mode voltage clamp (IDBFB-ACMVC) targets that interval. Two anti-series metal-oxide-semiconductor field-effect transistors (MOSFETs) and a 100 nF capacitor link the buck output with the DC-link midpoint, but only during the intervals when neither buck switch conducts. Their gate command is the logical NOR of the two buck gate commands, so the clamp requires no separate timing and never conducts load current. The design and its MATLAB/Simulink evaluation were reported in [25], where the clamp reduced the simulated leakage current from 18.6 mA to 3.8 mA RMS, and the transformerless topologies it is measured against were reviewed in [26]. This paper reports the hardware. Its contributions are:

1) A 1 kW prototype whose devices and gate drivers are matched to the reference node and switching rate of each of its eight switches, brought up in stages from a perfboard unfolding bridge to a single printed circuit board (PCB).
2) Measurements of efficiency from 250 W to 1 kW, voltage and current total harmonic distortion (THD), power factor and clamped common-mode ripple, and of leakage current with the clamp disabled and enabled in the same hardware.
3) A separation of the measured leakage current into the 100 Hz floor that the clamp cannot remove and the dead-time drift that it targets.
4) A comparison with published transformerless topologies on switch count, load-current path, leakage current, efficiency and THD.

Sections II to VII cover, in turn, the topology and clamp, the prototype, the measurement methods, the results, the comparison with simulation and published work, and the conclusions.

2. TOPOLOGY AND CLAMP PRINCIPLE

2.1 Power Stage

Figure 1 shows the circuit. Two 330 μF capacitors, C_1 and C_2, split the 380 V DC link and hold its midpoint M at $V_{\mathrm{PV}}/2 = 190$ V. Two buck legs, S_1-D_1-L_1 and S_2-D_2-L_2, switch at 40 kHz with carriers 180° apart and shape a rectified sine at their shared output node V_{buck}, with the duty cycle

$$D(t) = \frac{V_{g,\mathrm{pk}}\,|\sin(\omega t)|}{V_{\mathrm{PV}}} \tag{1}$$

where $V_{\mathrm{g,pk}} = 325.3$ V is the peak of the 230 V RMS output, $\omega = 2\pi \times 50$ rad/s, and V_{PV} is the DC-link voltage. The peak duty cycle is 0.856, so the buck stage never saturates, and interleaving doubles the ripple frequency at V_{buck} to 80 kHz.

The insulated-gate bipolar transistors (IGBTs) S_3 to S_6 unfold this waveform: S_3 and S_6 conduct in the positive half-cycle and S_4 and S_5 in the negative one, so the bridge switches only at the zero crossings. The output filter, $L_f = 0.5$ mH and $C_f = 4.7\,\mu$F, has its corner at 3.28 kHz and attenuates the 80 kHz ripple by about 55.5 dB. The design equations and the simulated behaviour are given in [25]; the relations needed to read the measurements are summarised below.

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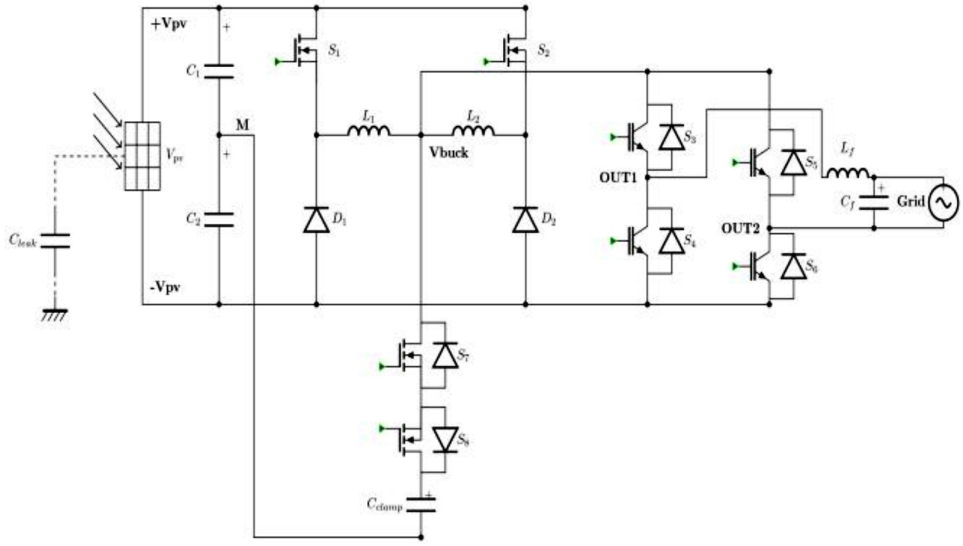


Fig. 1. Circuit of the IDBFB-ACMVC inverter. C_{leak} represents the PV-array capacitance to earth.

2.2 Common-Mode Voltage and Dead-Time Drift

With S_3 and S_6 on, output terminal A follows V_{buck} and terminal B sits at the DC negative rail; with S_4 and S_5 on, the roles reverse. In either state,

$$V_{\text{CM}} = \frac{V_A + V_B}{2} = \frac{V_{\text{buck}}}{2} \tag{2}$$

where V_A and V_B are the terminal voltages measured from the DC negative rail. A capacitance C_{leak} between that rail and earth therefore carries

$$I_{\text{leak}} = C_{\text{leak}} \frac{dV_{\text{CM}}}{dt} \tag{3}$$

While S_1 or S_2 conducts, V_{buck} is actively driven and V_{CM} follows only the 100 Hz envelope of (**??**). For $D(t) \leq 0.5$, however, the two legs leave two intervals in every 25 μs switching period in which S_1 and S_2 are both off, together lasting $[1-2D(t)]T_{\text{sw}}$, where T_{sw} is the switching period. This interval is called the dead-time here. V_{buck} is then left to whichever freewheeling diode conducts. D_1 and D_2 are never perfectly matched in forward voltage, so V_{buck} drifts by a few volts before settling, once in every switching period, and by (3) this drift dominates the leakage current when no clamp is present.

2.3 Clamp Branch and Control Law

The clamp (Figure 2a) joins S_7 and S_8 source to source, with the drain of S_7 at V_{buck} and the drain of S_8 at a node Y, and $C_{\text{clamp}} = 100$ nF connects Y

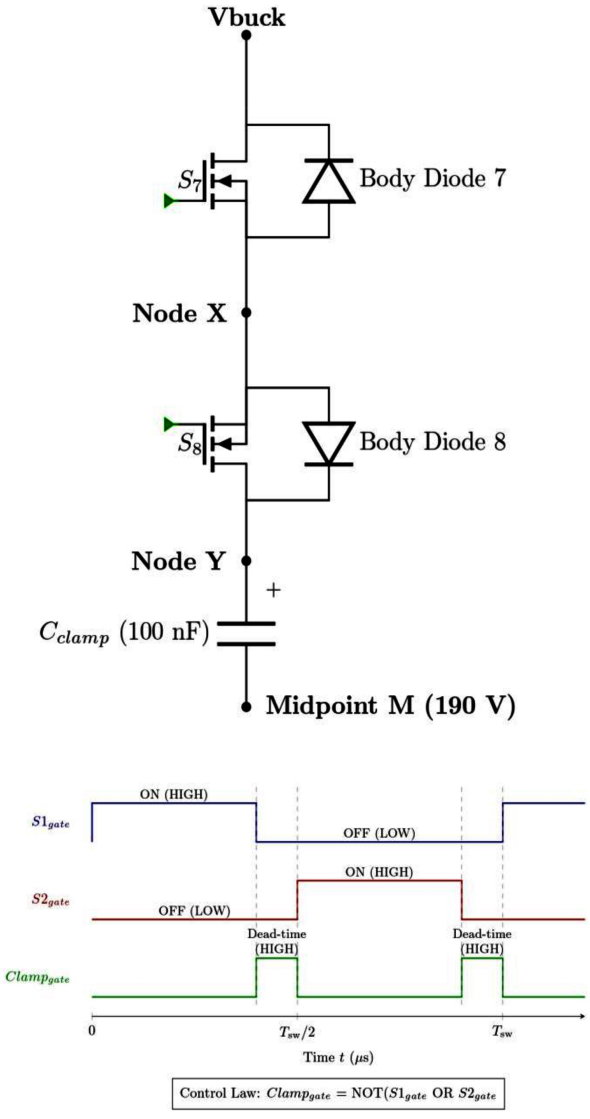


Fig. 2. (a) Active c_{clamp} branch: S7 and S8 in anti-series with c_{clamp} between V_{buck} and M. (b) Clamp gate derived from the buck gate signals by (4).

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to M. Because $V_{\text{buck}} - V_M$ changes sign twice in every half-cycle, a single MOSFET could not block it; the anti-series pair blocks both polarities when off and conducts in both directions when on. C_{clamp} in series blocks DC, so the clamp cannot shift the operating point of the buck stage and couples only the fast part of the drift. The gate signal is the NOR of the buck gate signals,

$$\text{Clamp}_{\text{gate}} = \text{NOT}(S1_{\text{gate}} \text{ OR } S2_{\text{gate}}) \tag{4}$$

which is high only while neither buck switch is commanded on (Figure 2b). The clamp is therefore active only in the dead-time, most often near the zero crossings, and silent wherever $D(t) > 0.5$, including the sine peak. With the $80\,\text{m}\Omega$ devices fitted (Section III), the clamp path has a time constant

$$\tau = \left(R_{\text{DS(on)},S7} + R_{\text{DS(on)},S8}\right) C_{\text{clamp}} = 16\,\text{ns} \tag{5}$$

So it settles in about 80 ns, short against both-off gaps of up to $12.5\,\mu$s, except near $D(t) = 0.5$, where the gap narrows to zero. Once engaged, the clamp shares the dead-time mismatch current between the parasitic capacitance C_{par} of the V_{buck} node and the much larger C_{clamp}, which scales the drift slope by

$$\frac{(dV_{\text{CM}}/dt)_{\text{clamped}}}{(dV_{\text{CM}}/dt)_{\text{unclamped}}} = \frac{C_{\text{par}}}{C_{\text{par}} + C_{\text{clamp}}} \tag{6}$$

about 0.01 for C_{par} of the order of 1 nF. Each clamp event moves only the charge needed to absorb a few-volt excursion, so the clamp loss is estimated at under 0.1 W.

The 100 Hz variation of V_{CM} is outside the clamp's reach. With $V_{\text{CM}} = \frac{V_{\text{g,pk}}}{2}\left|\sin \omega t\right|$, (3) gives a floor

$$I_{\text{leak,100 Hz}} = \frac{C_{\text{leak}} V_{g,\text{pk}}}{2} \frac{\omega}{\sqrt{2}} \tag{7}$$

equal to 3.6 mA RMS for $V_{\text{g,pk}} = 325.3$ V and $C_{\text{leak}} = 100$ nF. The floor and the drift occupy different frequency ranges, so their RMS values add in quadrature,

$$I_{\text{leak}} = \sqrt{I^2_{\text{leak,100 Hz}} + I^2_{\text{leak,drift}}} \tag{8}$$

where $I_{\text{leak,drift}}$ is the drift component. As the clamp removes the drift, the leakage current approaches the floor.

3. PROTOTYPE DESIGN AND IMPLEMENTATION

3.1 Ratings and Power Devices

Table 1. lists the ratings of the prototype and the parts fitted. The buck switches S_1 and S_2 are 650 V, 18 mΩ superjunction MOSFETs with a gate charge of 234 nC. At 40 kHz per leg, their switching loss outweighs their conduction loss, and the low on-resistance keeps the conduction share small.

The freewheeling diodes D_1 and D_2 are 650 V, 8 A silicon carbide (SiC) Schottky diodes with negligible reverse-recovery charge, so no recovery current flows through S_1 or S_2 when they turn on at the end of freewheeling; with silicon diodes, this loss would recur in every 40 kHz switching cycle.

The unfolding switches S_3 to S_6 are 1200 V trench field-stop IGBTs, whose loss at 50 Hz is conduction loss set by the collector-emitter saturation voltage, not switching loss. The clamp switches S_7 and S_8 are 600 V, 80 mΩ superjunction MOSFETs. Their gate charge of 51 nC is about a fifth of that of S_1 and S_2, and their continuous rating is 37 A against 106 A, because they carry only the clamp transient. C_{clamp} is a 100 nF, 630 V metallised polyester film capacitor, which holds its capacitance under the bipolar voltage across the clamp without the bias-dependent loss of capacitance of ceramic dielectrics.

3.2 Gate Drive and Control

A single Microchip dsPIC33 digital signal controller generates all eight gate commands; its independent pulse-width modulation (PWM) channel pairs time the 40 kHz buck legs and the 50 Hz bridge separately, and the clamp command follows the buck commands through (4).

Two rules fix the gate-driver choice (Table 2): the reference node of a switch decides whether isolation or bootstrapping is needed, and its switching rate decides which. S_1 and S_2 sit on a node that returns low every $25\,\mu$s, often enough to keep a bootstrap capacitor charged, so a half-bridge driver with an integrated bootstrap diode serves them.

S_3 and S_5 are also high-side switches, but each can remain on for an entire 10 ms half-cycle, much longer than a bootstrap capacitor can hold its charge, so they use optically isolated drivers with desaturation detection and an active Miller clamp. S_4 and S_6 sit on the fixed DC negative rail and need neither, so the ground-referenced low-side channel of a high-side/low-side driver drives them directly.

S_7 and S_8 float in the anti-series branch and switch on fast dead-time edges, so their isolated driver was selected for noise rejection rather than output current: its common-mode transient immunity

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Table 1. Ratings and components of the prototype.

Item	Rating or Part
Rated output power	1 kW
DC input	380 V, variac-fed rectifier bench supply
Output	230 V RMS, 50 Hz; 4.35 A RMS (6.15 A peak)
Buck stage	40 kHz per leg, 180° interleaved (80 kHz effective)
Unfolding bridge	50 Hz
S1, S2	IPW65R018CFD7, 650 V, 18 mΩ superjunction MOSFET
D1, D2	VS-3C08ET07T-M3, 650 V, 8 A SiC Schottky diode
S3 to S6	IGW40N120H3, 1200 V trench field-stop IGBT
S7, S8	IPW60R080P7, 600 V, 80 mΩ superjunction MOSFET
C1, C2	330 μF, 450 V, electrolytic
C_{clamp}	MMK15104K630B, 100 nF, 630 V DC, polyester film
L1, L2	2.0 mH, about 3 to 4 A, custom toroidal
L_f	0.5 mH, about 7 to 8 A, custom toroidal
C_f	F861FR475M310ZLH0J, 4.7 μF, 310 V AC, film
Controller	Microchip dsPIC33 digital signal controller
C_{leak} (test)	100 nF discrete capacitor, DC negative rail to earth

Table 2. Gate-driver arrangement.

Switches	Reference node	Driver and key ratings
S1, S2	Buck node, 40 kHz	2EDL05N06PF: bootstrap half-bridge, 600 V; source 0.36 A, sink 0.7 A.
S3, S5	Bridge high side, 50 Hz	ACPL-332J: optical isolation, 5 kV RMS, 2.5 A, desaturation detection, active Miller clamp.
S4, S6	DC negative rail, 50 Hz	UCC27714: ground-referenced low-side channel; 4 A.
S7, S8	Floating clamp branch; dead-time edges	Si8273BB-IS1: isolated, 2.5 kV; source 1.8 A, sink 4.0 A; CMTI ≥ 150 kV/μs.

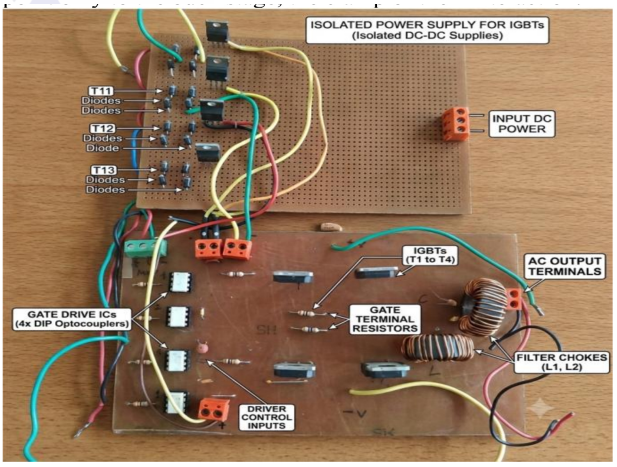
(CMTI) is at least 150 kV/μs, against a 15 kV/μs minimum for the optocoupler of S_3 and S_5.

3.3 Magnetics

L_1 and L_2 (2.0 mH, about 3-4 A) and L_f (0.5 mH, about 7-8 A) are the only custom-built passive components; L_f carries the combined output current, while L_1 and L_2 carry one leg's share each. For the development builds, toroidal cores were selected for the operating frequency and current, the wire gauge was set from the winding current, the number of turns was calculated as $N = \sqrt{\frac{L}{A_L}}$, where A_L is the inductance factor of the core, and each coil was wound by hand. The inductors of the final board were manufactured with the help of inductor-winding specialists to the same inductance values and current ratings.

3.4 Staged Bring-Up and Final Board

The prototype was brought up in stages, so that a fault on the integrated board could be traced to one stage. The unfolding bridge came first: a standalone H-bridge on perfboard with point - to - point wiring,



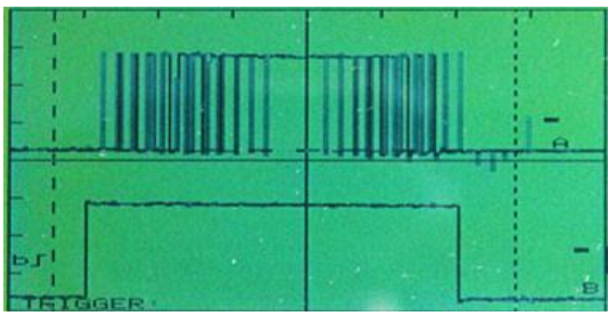


Fig. 3. Staged bring-up: (a) perfboard unfolding bridge with its TLP250 gate-driver board; (b) SPWM signals generated by the Arduino Uno for the bridge test.

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switched at 50 Hz before any high-frequency circuitry existed (Figure 3a). An Arduino Uno generated the sinusoidal pulse-width modulation (SPWM) pattern for this test (Figure 3b). Its 5 V outputs cannot drive an IGBT whose on-state voltage is specified at 15 V gate drive, so TLP250 optocouplers, one per switch and each rated ±1.5 A, translated the logic pulses into isolated gate drive. Neither the Arduino nor the TLP250 stage was carried onto the final board. Once the bridge and its drive behaved correctly on their own, a later fault could point only to the buck stage, the clamp or their interaction. The final board carries all stages on one PCB in a metal enclosure, arranged in five functional sections: the split DC-link bank, the unfolding bridge with its four IGBTs screw-mounted on a common heatsink, the dsPIC33 control section, the dual-buck and clamp section, and the output section with L_f and C_f. S_1, S_2, S_7 and S_8 share a second heatsink, with C_{clamp} in the same section, since the clamp gate derives from the buck gate signals.

4. TEST SET - UP AND MEASUREMENT METHODS

A variac-fed rectifier followed by a filter capacitor bank supplied the 380 V DC bus, holding it at a fixed, repeatable point for each measurement, which an array under changing irradiance would not. A 100 nF discrete capacitor between the DC negative rail and earth stood in for the parasitic capacitance of the array. It has the value of C_{leak} in the simulation of [25], so the simulated and measured leakage currents describe the same quantity.

The current through it was read on the milliampere range of an HTC DM-81 true-RMS multimeter, first with the clamp disabled and then with it enabled. An Aplab D37070A digital storage oscilloscope (DSO) with 70 MHz bandwidth and 1 GSa/s sampling recorded V_{buck} and V_{CM} through a 600 V differential probe.

V_{CM} was taken at the midpoint of a matched 100 kΩ divider across the output terminals, where the differential output cancels and only the common-mode component remains. DC and AC voltages and currents were read on true-RMS multimeters.

THD was computed by a fast Fourier transform (FFT) in Python from DSO waveforms exported as comma-separated values and summed to the 25th harmonic, in line with IEEE 519, so voltage and current use the same harmonic range whatever the instrument firmware would apply.

The power factor followed from the delay Δt between the zero crossings of output voltage and current,

$$\text{PF} = \cos\left(\frac{\Delta t}{T} \times 360^\circ\right) \tag{9}$$

where T is the fundamental period; the same acquisition supplied the THD records. Efficiency came from isolated Hall-effect voltage and current sensors read by an Arduino, which calculated true power, averaged over each cycle, at the DC input and AC output at the same time, something a true-RMS multimeter alone cannot do. These readings were cross-checked against the multimeter readings at each load point.

5. EXPERIMENTAL RESULTS

5.1 Steady-State Waveforms

The output voltage measured 696 V peak to peak over one 50 Hz cycle (Figure 4a), which corresponds to 246.1 V RMS for a sinusoid, about 7% above the 230 V nominal. The waveform repeats at the 50 Hz line frequency without visible drift. Vbuck over the same cycle (Figure 4b) is an unbroken rectified sine that peaks in the middle of each half - cycle and returns to near zero at each zero crossing, twice in

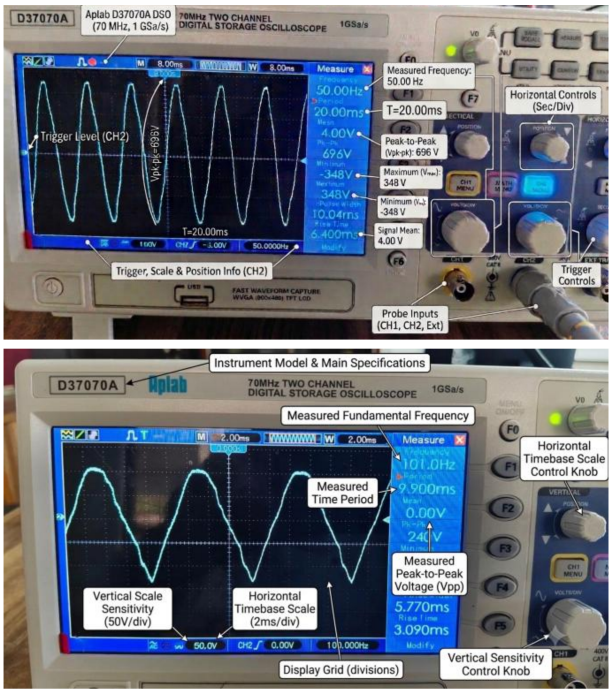


Fig. 4. Measured waveforms over one line cycle: (a) output voltage, 696 V peak to peak; (b) buck-stage output voltage V_{buck}.

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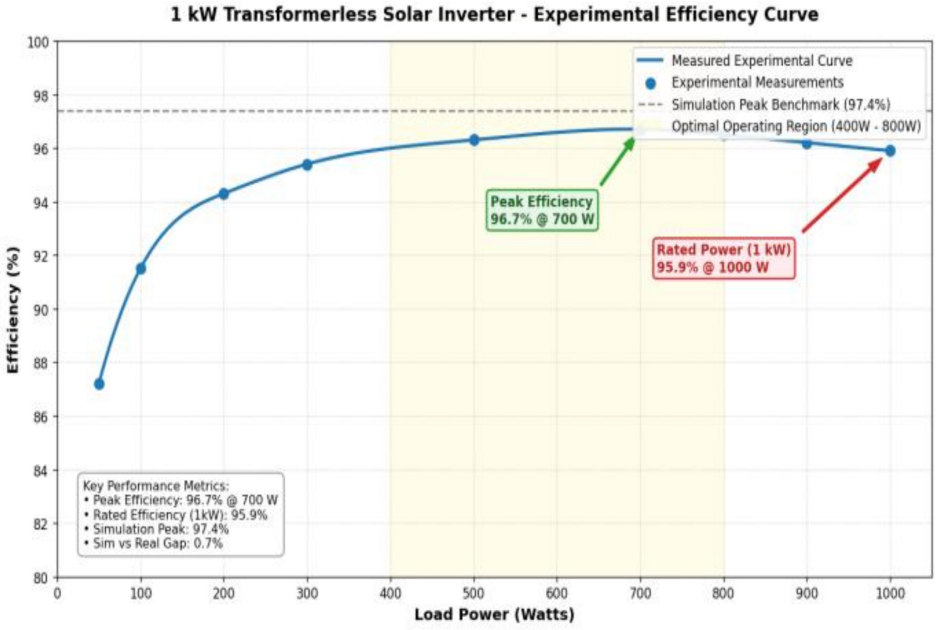


Fig. 5. Measured efficiency versus output power.

every 20 ms period. Steps or dead zones near the zero crossings would mark discontinuous conduction of the buck legs, and the capture shows none. The bridge reverses the output where this envelope is near zero, so S3 to S6 commutate at low voltage and low current.

5.2 Efficiency

Table 3 and Figure 5 give the efficiency at six load points. It rises from 94.9% at 250 W, where gate-drive, control-board and other largely load-independent losses weigh on a small output, to a peak of 96.7% at 700 W, then eases to 95.9% at 1 kW, where conduction loss in the buck MOSFETs, freewheeling diodes and unfolding IGBTs grows faster than the output. The dissipation, Pout(1 − η)/η, rises across the whole sweep. Between 700 W and 1 kW it grows by 79% for a 43% rise in output power, so rated load, not the efficiency peak, is where the devices run hottest. The simulated efficiency peaks at 97.4% near 700 W, essentially the load at which the hardware peaks, and is 97.24% at 1 kW [25].

5.3 Power Quality

The spectra computed from the exported waveforms (Figure 6) give a voltage THD of 1.99% and a current THD of 3.54%. The 13th harmonic, at 650 Hz, dominates both. The filter corner, at 3.28 kHz, lies far above 650 Hz, so the filter passes this component largely unattenuated without amplifying it. A harmonic of such low order points to dead-time-related nonlinearity in the line-frequency commutation of the unfolding bridge rather than in the 40 kHz buck legs. Both figures are inside the 5% limits of IEEE 1547-2018 for current [27] and of IEEE 519, as adopted in India, for voltage [28]. Current THD is the tighter of the two, a factor of 1.4 below its limit against 2.5 for voltage. The power factor exceeded 0.99, higher than the 0.90 minimum at half rated power that IEC 61727 sets, as reported in [29].

Table 3. Measured efficiency and dissipation.

Output (W)	Load (%)	Efficiency (%)	Loss (W)
250	25	94.9	13.4
500	50	96.3	19.2
700	70	96.7	23.9
750	75	96.6	26.4
900	90	96.2	35.6
1000	100	95.9	42.8

Loss is calculated as $P_{\text{out}}(1-\eta)/\eta$.

5.4 Leakage Current and Common-Mode Voltage

With the clamp disabled, the leakage current through the 100 nF test capacitor measured 46.4 mA RMS. With the clamp enabled in the same hardware it measured 9.6 mA RMS, a reduction of 79.3% (Figure 7). The unclamped figure exceeds 30 mA, the lowest disconnection threshold of VDE 0126-1-1 and the RCD rating that IEC 62109-2 allows [8, 9]. The clamped figure sits 3.1 times below that threshold and 31 times below the 300 mA continuous-leakage threshold [8].

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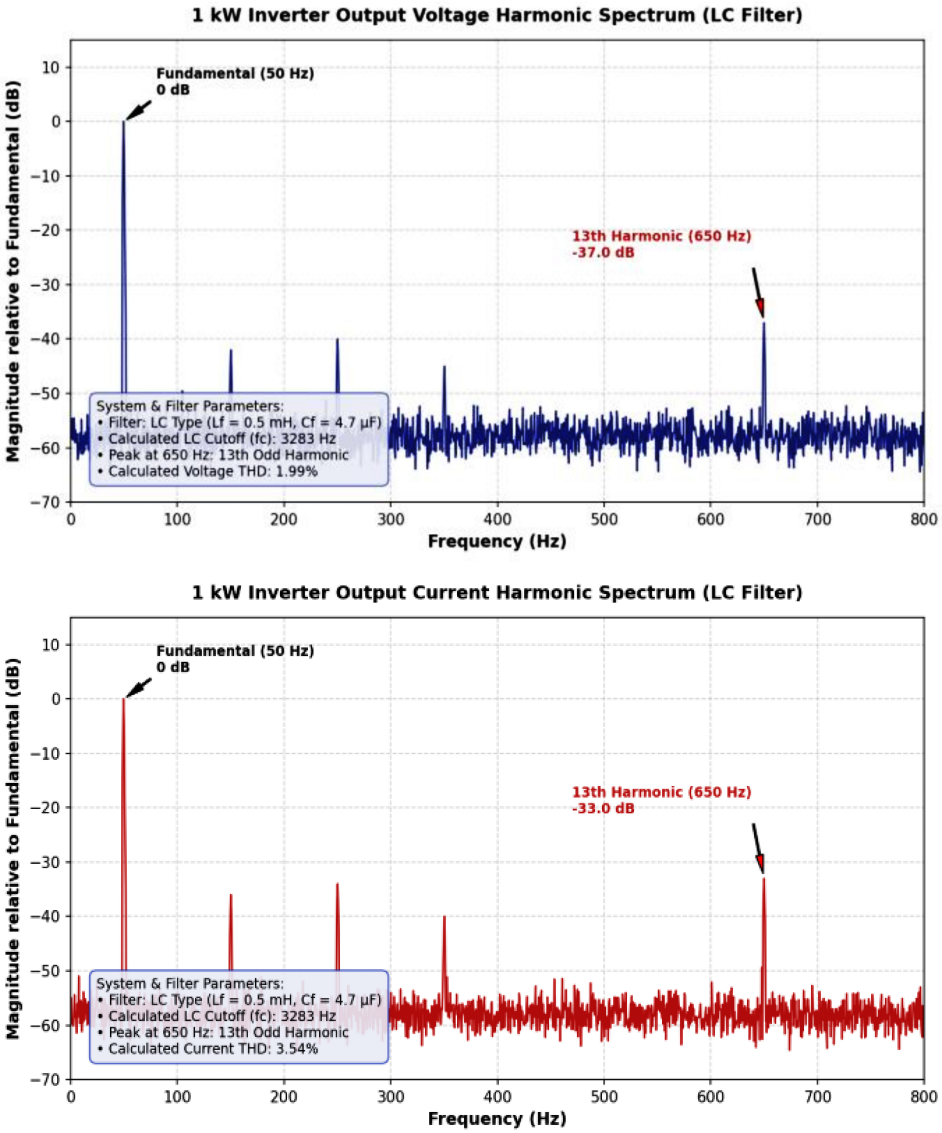


Fig. 6. (a) Harmonic spectra and THD calculated from the measured waveforms of the measured output voltage. (b) Harmonic spectra and THD calculated from the measured waveforms of the measured output current.

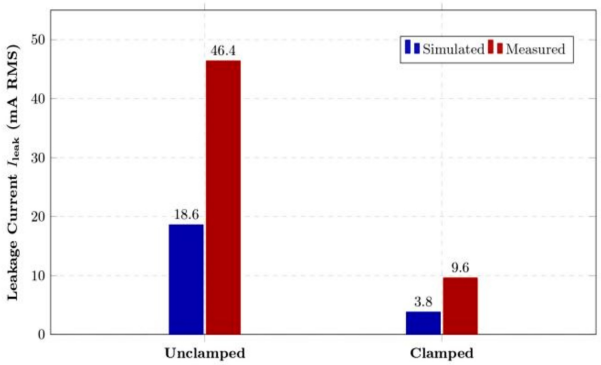


Fig. 7. Leakage current without and with the clamp: simulation [25] and measurement.

The common-mode ripple measured with the clamp active was 1.2 V peak to peak, while the simulation puts the unclamped swing at spikes of 3 to 5 V and the clamped ripple below 0.5 V [25]. The leakage current is this swing acting on Cleak through (3), so the voltage and current results are two views of the same suppression.

6. DISCUSSION

6.1 Simulation Versus Measurement

Table 4 sets the measurements against the simulation of [25]. The leakage reduction and the peak efficiency agree within one percentage point, absolute leakage runs about 150% above simulation, unclamped and clamped alike, and both THD figures rise while staying within their limits.

The absolute leakage gap follows from what the model leaves out. The simulation represents every path to earth by the single 100 nF Cleak, whereas a populated board adds capacitance between traces,

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Table 4. Simulated and measured performance.

Quantity	Simulated [25]	Measured	Deviation
Leakage, unclamped	18.6 mA	46.4 mA	+149.5%
Leakage, clamped	3.8 mA	9.6 mA	+152.6%
Leakage reduction	79.6%	79.3%	−0.3 pp
Peak efficiency (700 W)	97.4%	96.7%	−0.7 pp
Efficiency at 1 kW	97.24%	95.9%	−1.3 pp
Voltage THD	≈ 0.75%	1.99%	+1.24 pp
Current THD	≈ 1.8%	3.54%	+1.74 pp
Power factor	> 0.99	> 0.99	–
CM ripple, clamped	< 0.5 V p-p	1.2 V p-p	–

pp: percentage points; CM: common-mode.

planes and chassis. The two freewheeling diodes on the board also do not share the same forward drop, and neither matches the datasheet value used in simulation; that mismatch sets the size of the dead-time drift. The clamped figure is further raised by gate-driver propagation delay, which postpones the turn-on of S7 and S8 within each dead-time so the clamp covers slightly less of it, and by the stray inductance of the S7-S8-Cclamp loop, which slows the fast current the clamp relies on. The efficiency gap reflects device drops that spread around their datasheet values, the power drawn by gate drivers, sensors and the control board, and contact resistance, none of which a powerstage simulation includes. The THD rise is put down to deadtime distortion around the zero crossings, to filter tolerance that moves the corner away from its nominal 3.28 kHz and, for current, to sensor noise. These causes are inferred from circuit principles and were not measured separately. A gap of the same kind is reported for a two-stage dual-buck inverter, 0.2 mA in simulation against 12.3 mA measured once real devices replaced an ideal switch model [30]. The close agreement of the two reductions, 79.6% and 79.3%, hides a difference that (8) exposes. In simulation the floor of (7) is 3.6 mA, so the drift falls from 18.2 mA to 1.2 mA. The clamp removes more than 90% of it, and the clamped current lies within 0.2 mA of the floor, which caps the reduction. For the measured 246.1 V output, (7) gives a floor of 3.9 mA, and the drift falls from 46.2 mA to 8.8 mA, a removal of about 81%. The measured reduction is therefore limited mainly by the drift that remains rather than by the floor, and the near-equality of the two percentages is partly coincidental. Both results show the clamp removing most of the dead-time drift identified in Section II-B. On the attribution above, the drift that remains in hardware is the part set by gate-driver delay and clamp-loop inductance.

6.2 Comparison With Published Topologies

Table 5 compares the structure of the IDBFB-ACMVC with twelve published topologies, counting extra switches against a plain four-switch bridge.

Table 5. Structural comparison with published topologies.

Topology	Extra switches	In load path?	Control	Ref.
H5	+1	Yes	Low	[12, 31, 32]
HERIC	+2	Yes	Low	[12, 32]
H6 (DC-bypass)	+2, plus 2 diodes	Yes	Moderate	[12, 32–34]
oH5	+2, plus split capacitor	Yes	Moderate to high	[12, 17, 32]
NPC/Conergy NPC	+2 (diodes)	Yes	Low to moderate	[2, 18, 35]
ANPC	+2 (active)	Yes	High	[2, 36]
5L-DM-CGT	+5 (9 in all), plus 2 flying capacitors	Yes	High	[16]
HB-ZVR-D	+2 (diodes)	Yes	Low	[31]
CSI, 4-leg	+1 leg (2 switches)	Yes	Moderate	[37]
CSI, 6-switch	+2	Yes	Moderate	[38]
IDBFTI	+2	Yes	Low	[24]
SIDBFBI	+4	Yes	Low	[21]
IDBFB-ACMVC (present work)	+4 (2 buck, 2 clamp)	No	Low	–

ANPC: active NPC; 5L-DM-CGT: five-level dual-mode common-grounded-type; HB-ZVR-D: diode-clamped HB-ZVR; CSI: current-source inverter; IDBFTI: interleaved dual-buck full-bridge three-level inverter; SIDBFBI: single-inductor dual-buck full-bridge inverter.

The added devices range from the single series switch of H5 to the five extra switches (nine in all) and two flying capacitors of the common-ground five-level converter [16], and in every other topology the leakage-suppression element carries the full load current during part of the switching cycle. The IDBFB-ACMVC adds four switches, as many as SIDBFBI and towards the upper end of that range. S1 and S2 form the buck front end, and only S7 and S8 serve leakage suppression; they are the only suppression devices in the table that never carry load current. Its control complexity is low, since the clamp gate is a logic function of existing signals.

Table 6 compares the measured performance. Unclamped, the prototype leaks 46.4 mA, within 0.6 mA of H6 and 1.5 mA of oH5, and well below the 89.4 and 84.3 mA measured for H5 and HERIC [32]. Clamped, it is lower than all six measured variants of [40], which range from 12.84 to 29.19 mA, and within 0.07 mA of the simulated 9.67 mA of an improved H5 with its own common-mode clamp [39]. It does not reach the 3.5 and 2.5 mA of NPC and ANPC, both of which need a split DC bus of twice the voltage and a clamp leg that remains connected throughout the switching cycle [2]. Below 1 mA, [31] reports Conergy NPC on an 800 V bus and the Flying-Capacitor I/II and Siwakoti-H converters with a voltage THD of 4.2% to 4.3%, results not obtained on the same terms as this one.

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Table 6. Leakage current, efficiency and current THD.

Topology	Leakage (mA RMS)	η (%)	THD_I (%)
H5	89.4 [32]; 13.23 [31]	97.1† [12]	2.24† [12]
HERIC	84.3 [32]	96.8† [12]	0.88† [12]
H6 (DC-bypass)	45.8 [32]; 16.6–18 [34]	97.4† [12]	1.05–1.09† [12]
oH5	44.9 [32]	96.1† [12]	1.05–1.09† [12]
NPC/Conergy NPC	$\leq$ 3.5 [2]; $<$ 30† [35]	up to 98 [18]	1.45† [35]
ANPC	$\leq$ 2.5 [2]	97.64† [36]	n.r.
Improved H5, CM clamp [39]	9.67†	97.78†	0.68†
H6-D [40]	12.84	97.90	1.43
H6-I [40]	13.43	97.29	1.62
PN-NPC [40]	13.46	96.86	1.60
HBZVSCR [40]	13.94	95.26	1.80
HB-ZVR [40]	27.13	94.56	1.90
HERIC (Syed et al.) [40]	29.19	98.56	2.2
Present work	46.4 / 9.6	96.7	3.54

† Simulation result. Efficiency is the maximum value for [39, 40] and the present work, and as reported for the others. Present work: unclamped / clamped leakage. n.r.: not reported; PN-NPC: positive-negative NPC.

On maximum efficiency, the like-for-like basis, the prototype trails the HERIC, H6-D and H6-I results of [40] by 1.9, 1.2 and 0.6 points, leads HBZVSCR and HB-ZVR by 1.4 and 2.1 points, and is within 0.2 points of PN-NPC. Current THD is the one axis on which the comparison does not split: 3.54% is higher than every comparator in Table 6 that reports it, from 0.68% [39] to 2.24% for H5, although it remains inside the 5% limit. Of the topologies in Table 5, only the current-source inverters report higher measured current THD, 3.77% [38] and 5.9% [37].

6.3 Limitations

The evidence comes from one prototype operated from a fixed 380 V bus supplied by a variac-fed rectifier, with a discrete 100 nF capacitor standing in for the array, so array dynamics, maximum power point tracking and other input voltages were not tested. Because the front end steps down, the input must exceed the 325 V peak of the output, and a lower-voltage array would need a boost stage ahead of it. Each hardware result is a single measured point, not a statistical average. The leakage figures are RMS readings on a true-RMS multimeter, so the leakage waveform itself was not recorded, and the efficiency figures rest on the Hallsensor chain cross-checked against multimeter readings. Device case temperatures were checked with an infrared thermometer at rated and near-rated load only, and no temperature readings are reported. The suppression was not swept against Cclamp or the clamp-path resistance, and the causes assigned to the deviations in Table 4 are inferred, not measured.

7. CONCLUSION

In a 1 kW IDBFB-ACMVC prototype tested from a 380 V DC bus, a clamp of two anti-series 80 mΩ MOSFETs and a 100 nF film capacitor, gated by the NOR of the two buck gate signals, cut the measured leakage current from 46.4 mA to 9.6 mA RMS (79.3%), 3.1 times below the 30 mA threshold of VDE 0126-1-1, without adding a device to the load-current path or a PWM channel. Efficiency peaked at 96.7% at 700 W and was 95.9% at 1 kW, voltage and current THD were 1.99% and 3.54%, and the power factor exceeded 0.99. Against simulation, the leakage reduction and the peak efficiency agree within one point, while absolute leakage runs about 150% higher. Separating the leakage into its 100 Hz floor and its dead-time drift shows that the clamp removes about 81% of the drift in hardware and more than 90% in simulation. Among published topologies, the clamped leakage is lower than that of H5, HERIC, H6, oH5 and all six variants of [40] but higher than that of NPC and ANPC and the sub-1 mA results of [40], which were obtained on different terms, and current THD is the weakest result. A sweep of Cclamp and the clamp-path resistance, an output filter redesigned for lower current THD, and tests from a PV array at other input voltages and power ratings are the next steps.

DECLARATIONS

Ethical Approval

We affirm that this manuscript is an original work, has not been previously published, and is not currently under consideration for publication in any other journal or conference proceedings. All authors have reviewed and approved the manuscript, and the order of authorship has been mutually agreed upon.

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research and findings presented in this paper. The authors alone are responsible for the content and writing of this article.

Authors' contributions

All authors contributed equally in the preparation of this manuscript.

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