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RESEARCH ARTICLE

Design and Analysis of an Interleaved Dual - Buck Full - Bridge Transformerless Inverter with Active Common-Mode Voltage Clamp for Photovoltaic Applications

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ABSTRACT: Transformerless photovoltaic (PV) inverters have emerged as the preferred solution for grid-connected residential and commercial systems owing to their reduced size, lower cost, and improved efficiency achieved by eliminating the line-frequency transformer. However, the absence of galvanic isolation introduces common-mode (CM) leakage current through the parasitic capacitance between the PV array and the grounded module frame, leading to safety concerns, electromagnetic interference, and reduced system reliability. This paper presents the design and analysis of an interleaved dual-buck full-bridge (IDBFB) transformerless inverter incorporating an active common-mode voltage clamp (ACMVC) to mitigate residual CM voltage and suppress leakage current. The proposed topology employs two interleaved buck converters operating at 40 kHz for high-frequency power processing, while a 50 Hz unfolding full-bridge generates the grid-frequency AC output, thereby inherently reducing CM voltage variations. To eliminate the residual CM voltage generated during buck-converter dead-time intervals, an ACMVC comprising two back-to-back MOSFETs, a blocking capacitor, and a simple NOR-gate-based control circuit is introduced to clamp the buck-output node to the DC-link midpoint. A 1 kW, 230 V RMS, 50 Hz prototype system is designed and modelled in MATLAB/Simulink to evaluate the proposed control strategy. Simulation results verify correct PWM generation, interleaved converter operation, synchronized unfolding-bridge switching, and effective clamp activation during dead-time intervals, demonstrating the feasibility of the proposed approach for reducing common-mode disturbances. The presented work establishes a practical design framework for transformerless PV inverters and provides a foundation for future experimental validation of leakage current, total harmonic distortion, conversion efficiency, and compliance with grid-interconnection standards.

Keywords: Active Clamp; Common-Mode Current; Grid-Connected Inverter; Interleaved Dual-Buck Converter; Leakage Current; Photovoltaic; Transformerless Inverter.

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1. INTRODUCTION

1.1 Market Context and Motivation

Grid - connected photovoltaic (PV) generation has expanded rapidly, making the power electronic inverter a critical interface between the PV array and the utility grid. As PV penetration increases, inverter efficiency, power density, reliability, and grid-interconnection performance have become key design considerations [1–3]. Traditional inverter topologies employed line-frequency transformers to provide galvanic isolation between the PV array and the grid. However, these transformers introduce additional size, weight, cost, and power losses

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into the conversion system [4]. Transformerless inverter architectures eliminate the bulky isolation transformer, enabling higher conversion efficiency, reduced system weight, and lower overall system cost [1, 3, 4].

Consequently, these topologies have received widespread attention for single-phase grid-connected residential and commercial PV applications [1, 2, 5]. However, the removal of galvanic isolation introduces a significant technical challenge: the parasitic capacitance between the PV array and ground provides a path for leakage current. This leakage current is strongly influenced by the common-mode voltage generated by the inverter topology and its modulation strategy. Therefore, effective common-mode-voltage mitigation is essential for ensuring safe and reliable operation of transformerless PV inverters [2, 3, 5].

1.2 The Leakage-Current Problem

A typical crystalline-silicon PV module mounted on a grounded aluminum rack exhibits parasitic capacitance to the supporting frame in the range of 50–300 nanofarads per kilowatt of installed capacity [6]. When the inverter produces time-varying common-mode (CM) voltage-defined as the average of the output terminals referenced to the negative DC rail-displacement current flows through this capacitance:

$$I_{\text{leak}} \approx C_{\text{PV}} \cdot \frac{dV_{\text{cm}}}{dt}. \quad (1)$$

The leakage current has three primary consequences. First, it can trip residual-current circuit interrupters (RCCIs) and residual-current devices (RCDs) designed to detect genuine ground faults. Because protective devices are sized for fault currents in the range 10-30 mA RMS, unmitigated inverter leakage at 50-100 mA RMS can cause nuisance disconnection, reducing inverter availability and grid reliability. Second, the high-frequency content of leakage current contributes both conducted and radiated electromagnetic emissions, potentially violating limits set by IEC 61000 and EN 55011 [7]. Third, under certain fault scenarios, leakage current can create a touch-hazard at exposed conductive parts, introducing personal safety concerns [8].

Standards have responded with explicit limits. The German standard VDE 0126-1-1 (now harmonized into IEC 62109-2) sets a 300 mA RMS continuous disconnection threshold, but much tighter trip thresholds at lower currents: any current step exceeding 30 mA must be cleared within 300 ms, and a 100 mA step must clear within 50 ms [9]. This means the practical leakage-current budget for a well-designed inverter is governed by the fast-trip tiers, not the headline 300 mA figure. In installations with multiple parallel inverters or sensitive loads, the effective budget becomes even tighter because leakage currents superpose.

1.3 Existing Mitigation Topologies

The standard remedies for transformerless inverter leakage current fall into two families, both based on the principle of clamping the CM voltage during inverter dead-time or freewheeling intervals when high-frequency switching would otherwise produce sharp CM transients.

The H4-derived family (H5, HERIC, H6, and variants) starts with a conventional full-bridge (H4) topology that switches at tens of kilohertz. High-frequency modulation of the H4 bridge produces large CM voltage swings (often ±300 V to ground in a single half-cycle), leading to uncontrolled leakage currents of 100-300 mA RMS [10]. These topologies add extra switches to interrupt the PV-to-grid connection during freewheeling intervals:

H5: Single DC-side series switch blocks the array during freewheeling [11].
HERIC: AC-side bypass leg provides a current path without forcing array voltage to track the bridge [12].
H6 variants: Multiple switches enable multiple freewheelingmodes, further reducing CM excitation [13, 14].

All H4-family solutions reduce leakage current by 80-95% (from hundreds of mA to tens of mA) but at the cost of added devices, gate-drive complexity, and continuous conduction loss through extra switches carrying the full inverter output current.

The dual-buck inverter family follows a fundamentally different approach [6, 15]. Instead of modulating a full bridge at high frequency, it uses two interleaved buck converters to shape a rectified sinusoidal intermediate waveform, then unfolds that waveform into AC using a bridge operating at only the grid frequency (50 Hz). Since the PV array connects to the buck stage rather than to a high-frequency AC bridge node, the array is not directly exposed to rapid CM voltage transitions. Baseline leakage current is therefore much lower than any H4-family design-typically 10-20 mA RMS-because the dominant source of CM excitation is simply absent.

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1.4 The Residual Problem and Proposed Solution

Despite the dual-buck topology's favorable baseline, a second-order effect remains. During the brief interval (≈500 ns) when both buck switches are simultaneously off, the buck-output node is undriven and left floating. Small mismatches in freewheeling diode forward voltage and device junction capacitance allow that node to drift by a few volts. Because this drift occurs over a very short time, the derivative dV_{cm}/dt is large (equation 1), producing sharp leakage-current spikes of 30-40 mA peak-concentrated at dead-time events-even though the baseline (time-averaged) leakage is much lower than from an H4-family design.

This paper proposes an active common-mode voltage clamp (ACMVC) to suppress that residual drift. The clamp consists of two small MOSFETs connected back-to-back, a single blocking capacitor, and gate-drive logic implemented as a simple NOR operation applied to the two buck gate signals. By connecting the buck-output node to the DC-link midpoint only during the simultaneous off-state of both buck switches, the clamp suppresses dV_{cm}/dt during precisely the interval where it would otherwise be largest. The approach is proportionate to the problem: rather than adding full-voltage switches in the main power path (as H4-family topologies do), the clamp adds only two low-voltage devices that conduct for microseconds per switching cycle.

1.5 Paper Contributions and Organization

The main contributions of this work are:

1. A detailed theoretical analysis of the CM voltage mechanism in dual-buck inverters, identifying the dead-time floating-node condition as the dominant source of residual leakage current.

2. A simple, cost-effective active clamp topology: two back-to-back MOSFETs plus a blocking capacitor, gated using only the buck gate signals already present in the controller's logic.

3. A complete 1 kW, 230 V RMS, 50 Hz reference design with detailed component selections.

4. A correction to the original IDBFB circuit specification regarding unfolding-bridge IGBT device

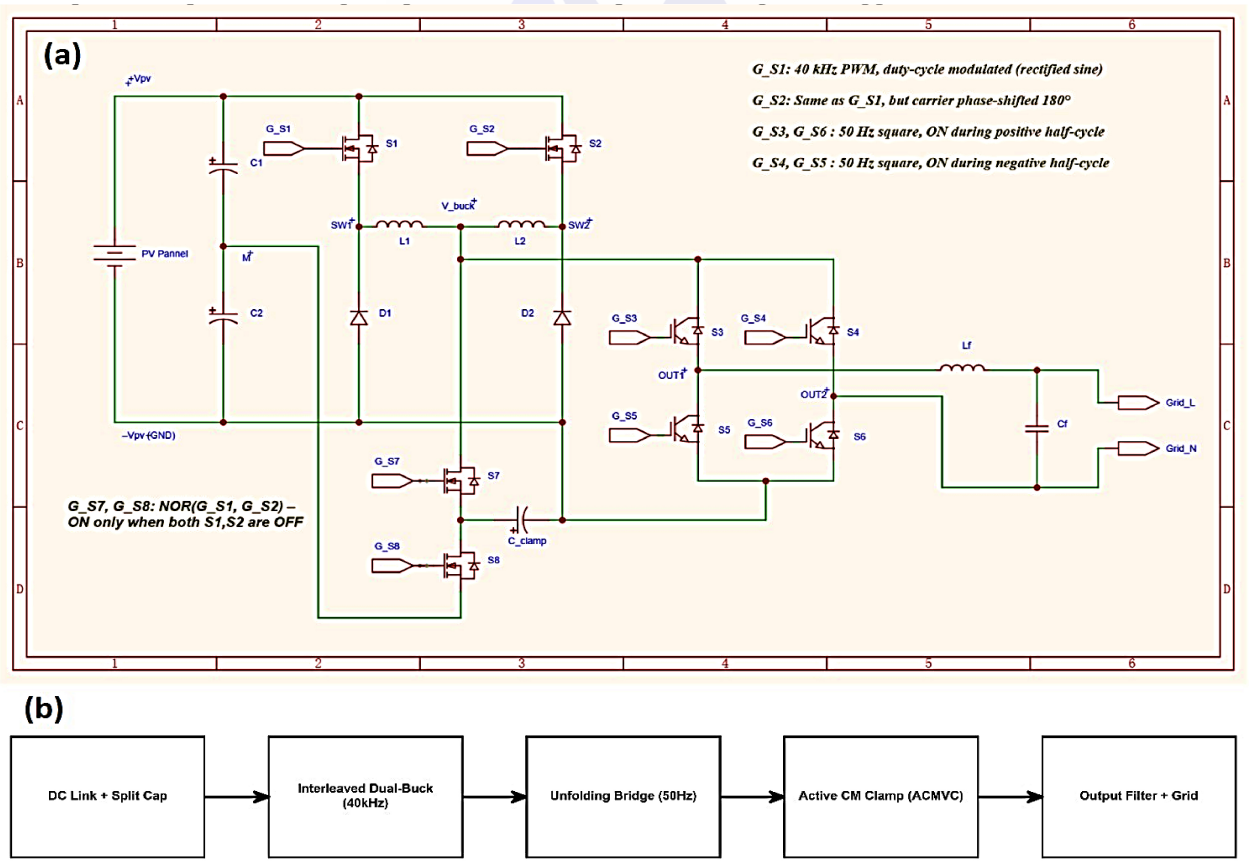


Fig. 1. (a): Complete IDBFB Inverter Schematic Diagram with ACMVC and (b) System Architecture Block Diagram of Proposed IDBFB.

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Table 1. Comparison of transformerless PV inverter topologies in terms of PV exposure, additional switches, leakage current, and dominant loss mechanisms.

Topology	Fast-switching stage sees PV directly?	Extra switches vs. baseline H4	Typical leakage-current (unmitigated)	Dominant loss-mechanism
H4 [11] (baseline)	Yes	–	hundreds of mA, often exceeds 300 mA RMS	Bridge switching loss
H5 [11]	Yes, briefly	1 (DC-side)	tens of mA	Added series-switch conduction loss
HERIC [12]	Yes, briefly	2 (AC-side)	tens of mA	AC bypass leg conduction loss
H6 [13, 14]	Yes, briefly	2	single-digit to tens of mA	Extra device conduction loss, partially offset by reduced bridge loss
Dual-buck / IDBFB [6, 15, 16]	No (only buck stage)	0 vs. baseline dual-buck; bridge itself switches at 50 Hz	10-20 mA (residual dead-time drift only)	Buck-stage switching loss (interleaving mitigates this)
IDBFB + ACMVC (proposed)	No	2 small MOSFETs + 1 capacitor	< 4 mA	Buck-stage switching loss; clamp loss negligible

selection, emphasizing the necessity of integrated antiparallel diodes for inductive loading.

5. MATLAB/Simulink behavioral verification of the complete control architecture, gate-drive timing, and waveform generation, establishing feasibility for laboratory prototyping.

6. A rigorous comparison between the dual-buck-plus-clamp approach and competing H4-family topologies, clarifying the distinct advantages and trade-offs of each family.

The remainder of this paper is organized as follows. Section II surveys related topologies and clarifies where the dual-buck approach sits relative to existing leakage-current mitigation strategies. Section III develops the circuit topology in detail, including the baseline IDBFB architecture, the unfolding bridge, the active clamp circuit, and the output filter. Section IV analyzes the common-mode voltage behavior and derives the mathematical relationship between CM drift and leakage current. Section V specifies the 1 kW design and lists all component selections with design rationale. Section VI describes the MATLAB/Simulink model and presents simulation results. Section VII discusses practical implementation considerations, including design margins, trade-offs, and scenarios where the clamp provides the most value. Section VIII concludes and outlines directions for future experimental validation.

2. RELATED WORK AND TOPOLOGY COMPARISON

2.1 A. Transformerless Inverter Topologies: A Structured Review

Transformerless PV inverters are often discussed as a homogeneous family, but they employ distinct strategies to achieve leakage-current reduction. A systematic comparison reveals important differences in baseline leakage mechanisms, added complexity, and practical applicability.

2.1.1 The H4 Baseline

The conventional full-bridge (H4) topology uses four IGBTs arranged in two legs, with the midpoint of each leg tied to one of the output terminals. The bridge switches at tens of kilohertz (typically 16-20 kHz), and the duty cycle modulation produces a PWM voltage waveform at the output. An LC filter smooths the PWM into a sinusoid. The critical problem is that both PV terminals are directly exposed to this high-frequency switching. The positive and negative rails swing through large voltages at the switching frequency, creating CM voltage variations of ±300 V or larger in a single transition. These sharp transients drive displacement current through the array-to-ground capacitance, producing leakage currents of 100-300 mA RMS [10]-well above the thresholds for protection-device nuisance tripping.

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2.1.2 H5 Topology [11]

Adds one series MOSFET on the positive DC rail (between the PV positive and the full bridge). During the bridge's freewheeling intervals (when all four bridge switches are off and current recirculates through the antiparallel diodes), the series switch is also turned off, disconnecting the PV from the bridge. This prevents the PV voltage from being pulled along by the bridge's transient behavior. Leakage current drops to 20-50 mA RMS. The cost is continuous conduction loss through the series switch on every cycle: a 1 kW inverter at 300 A rated DC input sees approximately 4.3 W of loss in a 48 mΩ switch. The gate-drive requirement is also slightly more complex, as the series switch's timing must be coordinated with the bridge's dead times.

2.1.3 HERIC Topology [12]

Instead of a DC-side series switch, HERIC adds an AC-side bypass branch. The bypass leg provides a freewheeling path for the inverter output current without forcing the PV voltage to follow the bridge. This distributes the added conduction loss (now in the bypass switching leg rather than a series switch) and can reduce the peak device current in some conditions. Leakage current is comparable to H5 (20-50 mA RMS). Complexity is similar but the added bypass switches must handle the full inverter current, so device sizing is still substantial.

2.1.4 H6 Family [13, 14]

These topologies introduce additional switches (typically two or three more than H4) to enable multiple freewheeling modes. By carefully selecting which switches are active during different parts of the grid cycle, H6 designs can reduce both peak CM excursion and average leakage current to single-digit millimeters (5-20 mA RMS). The trade-off is increased switching complexity and additional gate-drive channels. Some loss benefit may be gained if the extra switches are used to reduce bridge conduction loss in specific modes, but this must be carefully optimized.

2.1.5 Dual-Buck Topology [6]

Fundamentally different strategy. Instead of trying to control the CM voltage produced by a high-frequency bridge, the topology avoids producing large CM swings in the first place. Two buck converters (operating at 40 kHz, often interleaved) shape the output into a rectified sinusoidal envelope. A separate full bridge, switching at only 50 Hz, provides polarity unfolding. Because the PV array attaches only to the buck stage, not the bridge, the array voltage is quiet except during the z

2.2 Key Insights from Comparison

Three observations follow from Table 1:

First, the leakage-current baseline for the dual-buck topology is inherently better than any H4-family design because the fundamental source of CM excitation-a high-frequency AC bridge connected to the PV array-is absent. This is not an active clamp or a disconnection switch; it is a structural advantage that emerges from how the topology partitions the power-conversion task.

Second, the residual leakage in a dual-buck design (10-20 mA RMS) is qualitatively different from what H4-family topologies face. It is not a broad-spectrum high-frequency disturbance but rather localized sharp spikes concentrated at the brief intervals when the buck-output node is floating. This narrow problem admits a narrow, proportionate solution.

Third, the added complexity of the dual-buck front-end (two interleaved buck stages instead of a single H4 bridge) is offset by the simplicity of the unfolding-bridge stage (50 Hz operation rather than 16-20 kHz). The net control complexity is comparable to H4, and the power-conversion efficiency is typically 1-2 percentage points better because the buck stages operate at inherently lower loss than a PWM bridge.

3. CIRCUIT TOPOLOGY AND DETAILED OPERATING PRINCIPLES

3.1 System Architecture Overview

The proposed inverter system is organized into five functional blocks (Figure 1):

1. **DC-Link Supply and Split Capacitor Bank** Establishes the intermediate DC voltage and provides a midpoint reference.
2. **Interleaved Dual-Buck Converter Stage** Shapes the DC input into a rectified sinusoidal waveform at twice the grid frequency.
3. **Line-Frequency Unfolding Full Bridge** Converts the rectified waveform into a true AC waveform by alternating polarity.
4. **Active Common-Mode Voltage Clamp** Suppresses residual CM disturbances during buck dead-time intervals.
5. **Output Filter and Grid Connection** Attenuates high-frequency ripple and couples the inverter to the utility grid.

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The five functional blocks are present: DC-link, buck stage, unfolding bridge, clamp, and output filter.

3.2 DC-Link and Split Capacitor Bank

3.1.1 Design Considerations

The photovoltaic array is modeled as a DC voltage source. For grid-connected operation at 230 V RMS, the required DC-link voltage must exceed the grid peak voltage:

$$V_{\text{peak}} = \sqrt{2} \times V_{\text{grid,rms}} = \sqrt{2} \times 230 \approx 325\,\text{V}$$

In a pure buck converter architecture (where output voltage ≤ input voltage), the DC-link voltage must therefore be at least 325 V to permit the inverter to generate a 230 V RMS output with control margin. In practice, a 320 V DC-link voltage (used in some literature) is marginal. A more realistic design target is 380–400 V, achievable either by:

• Sizing the PV array to naturally operate at 380–400 V (common for residential systems).
• Using a front-end boost converter if the array operates at lower voltage.

A 400 V DC-link provides comfortable headroom for control transients and filter-stage voltage drops.

3.1.2 Split Capacitor Architecture

The DC link is divided into two series capacitors, C_1 and C_2:

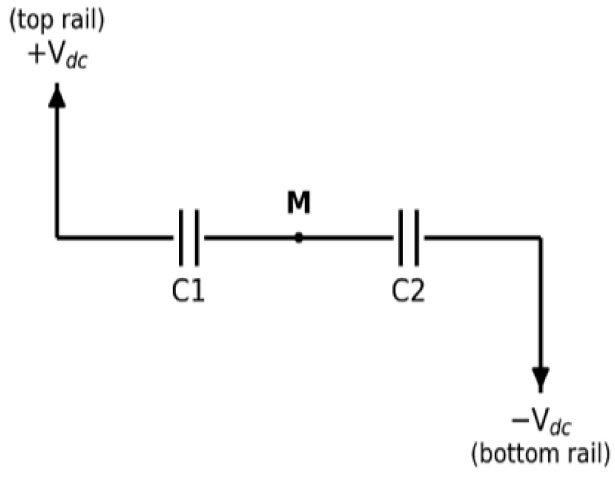


Fig. 1-1. Split DC-Link Capacitor Configuration with Midpoint Reference.

Both capacitors are 330 µF, 450 V (TDK B43644 series).

The junction M is the midpoint, with:

$$V_M = \frac{V_{\text{dc}}}{2} = 160\,\text{V} \quad (\text{if } V_{\text{dc}} = 320\,\text{V})$$

or

$$V_M = 190\text{-}200\,\text{V} \quad (\text{if } V_{\text{dc}} = 380\text{-}400\,\text{V})$$

The split-capacitor architecture serves two purposes:

a) It establishes a stable reference node M at half the DC-link voltage by virtue of symmetry. If both capacitors are identical and carry the same current waveform, their voltages are inherently balanced.

b) It provides the reference point for the active clamp and the conventional definition of CM voltage in transformerless inverter analysis.

To maintain voltage balance under transient and asymmetric current conditions, 47 kΩ balancing resistors can connected in parallel with each capacitor. These resistors provide a high-impedance DC path that equalizes any small voltage imbalances over time constants of milliseconds.

3.3 Interleaved Dual-Buck Converter Stage

3.3.1 Fundamental Operation:

The dual-buck stage comprises two identical buck converter legs:

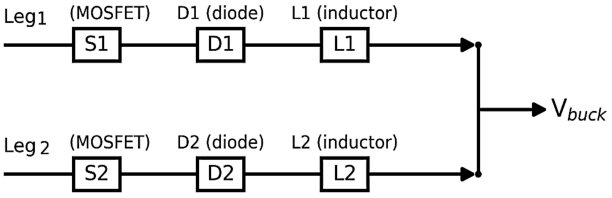


Fig. 1-2. Interleaved Dual-Buck Converter Stage Topology.

Both legs' outputs are tied to a shared node, Vbuck. Each MOSFET is driven using the same duty-cycle reference, which is a rectified 50 Hz sinusoid:

$$d(t) = |\sin(2\pi \cdot 50\,\text{Hz} \cdot t)| \tag{2}$$

The duty cycle varies from 0 (at t = 0, 10, 20, ... ms) to 1 (at t = 5, 15, 25, ... ms) and back to 0, tracing the absolute value of one full grid cycle. This rectified envelope synchronizes the buck output to the grid frequency and amplitude.

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3.3.2 Interleaving Strategy:

The critical innovation is that while both legs use the same duty-cycle reference, they are driven by two PWM carriers that are phase-shifted by 180°:

$$\text{Carrier}_1(t) = \text{sawtooth}\left(2\pi \cdot 40\,\text{kHz} \cdot t\right).$$

$$\text{Carrier}_2(t) = \text{sawtooth}\left(2\pi \cdot 40\,\text{kHz} \cdot t + \pi\right)$$
$$= \text{sawtooth}2\pi \cdot 40\,\text{kHz}\left(t - 12.5\,\mu\text{s}\right)$$

The gate signals are generated by comparing the duty-cycle reference against each carrier:

$$S_1 = (d(t) > \text{Carrier}_1)$$

$$S_2 = (d(t) > \text{Carrier}_2)$$

Because the carriers are 180° out of phase, the pulses in S_1 and S_2 are staggered. When S_1 is in the middle of its on-time, S_2 is typically near its off-time (or vice versa). This staggering is the essence of interleaving.

3.3.3 Ripple Cancellation

Each inductor has its own ripple current:

$$I_{L1}(t) = I_{L1,\text{avg}} + \Delta I_{L1} \sin\left(2\pi \cdot 40\,\text{kHz} \cdot t + \phi_1\right)$$

$$I_{L2}(t) = I_{L2,\text{avg}} + \Delta I_{L2} \sin\left(2\pi \cdot 40\,\text{kHz} \cdot t + \phi_2\right)$$

If the two legs were identical and the duty cycles identical, the ripple components would have:

$\varphi_2 \approx \varphi_1 + 180°$

The total current at V_{buck} would be:

$$I_V(\text{buck}) = I_{L1} + I_{L2} \approx 2I_{\text{avg}} +$$

$$\Delta I\left[\sin(\cdots + \phi_1) + \sin(\cdots + \phi_1 + 180°)\right]$$

The two ripple sine waves add to nearly zero (they are approximately 180° out of phase and equal in amplitude), leaving:

$$I_V(\text{buck}) \approx 2I_{\text{avg}} +$$

(small residual ripple at $2 \times 40\,\text{kHz} = 80\,\text{kHz}$)

The ripple frequency at the shared node effectively doubles to 80 kHz, and the peak-to-peak magnitude decreases significantly. This reduces the filtering burden on the downstream LC filter. PWM signal is generated comparing Rectified sinusoidal duty-cycle reference at one instant and two triangular carriers phase-shifted by 180°. Resulting gate signals S_1 and S_2, staggered in time. Note the 500 ns dead-time insertion between all transitions to prevent shoot-through.

The envelope follows the rectified sine, reaching 325 V peak at the grid zero-crossing points. High-frequency 80 kHz ripple is visible but at small amplitude due to interleaving.

Note the 180° phase offset between the ripple components. The sum I_{L1} + I_{L2} = $I_{V(buck)}$ (green) shows minimal 40 kHz ripple due to cancellation; the residual ripple is at 80 kHz.

3.3.4 Selecting Inductance Value

The inductance sets the peak-to-peak current ripple

$$\Delta I_{\text{pp}} = \frac{V_{\text{dc}} D(1-D)}{f_{\text{sw}} L}. \tag{3}$$

where D is the duty cycle (varying from 0 to 1 across the half-cycle) and f_{sw} = 40 kHz. For a 2 mH inductor at 40 kHz switching and with D varying between 0 and 0.8 (bounded by the requirement that output voltage ≤ input voltage), the peak ripple at maximum is roughly:

$$\Delta I_{\text{pp}} \approx \frac{400\,\text{V} \times 0.5 \times 0.5}{40\,\text{kHz} \times 2\,\text{mH}} \approx 1.25\,\text{A}$$

At 4.35 A RMS output (1 kW at 230 V), the ripple-to-average ratio is moderate. The choice of 2–5 mH represents a trade-off: smaller inductances reduce size and cost but increase ripple (requiring heavier output filtering); larger inductances smooth the output but add size and cost.

3.4 Unfolding Full Bridge

3.4.1 Operational Principle

The buck output is a rectified sine: it oscillates from 0 V to 325 V at twice the grid frequency. To convert this one-directional waveform into a true AC waveform that swings positive and negative, a full bridge is used:

During the positive grid half-cycle (0–10 ms):

- S_3 and S_6 are ON; S_4 and S_5 are OFF.
- OUT1 = V*buck* (positive).
- OUT2 = 0 V (negative rail).
- Output voltage = OUT1 − OUT2 = V*buck* (positive).

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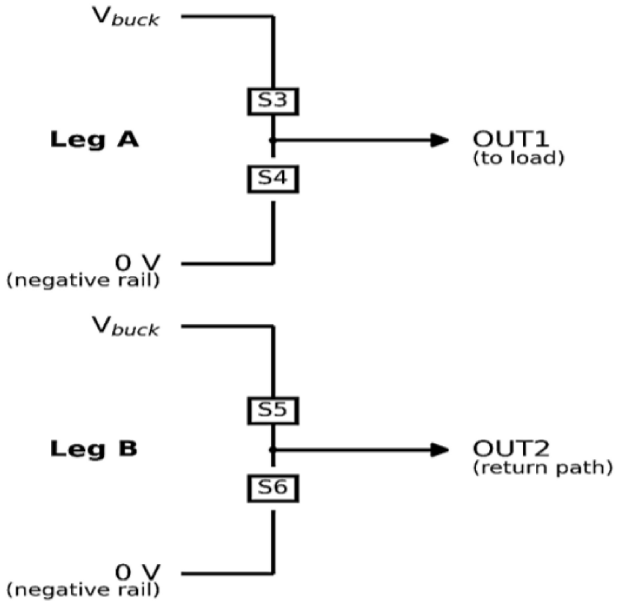


Fig. 1-3. Line-Frequency Unfolding Full-Bridge Circuit Diagram.

During the negative grid half-cycle (10–20 ms):

• S_4 and S_5 are ON; S_3 and S_6 are OFF.
• OUT1 = 0 V.
• OUT2 = V*buck* (positive).
• Output voltage = OUT1 − OUT2 = −V*buck* (negative).

By switching the bridge configuration at the grid zero crossing, the polarity of the output is reversed every half-cycle, converting the rectified input into a true AC waveform.

3.4.2 Critical Device Selection: Unfolding Bridge IGBT Choice

An often-overlooked practical issue arises from the inductive output filter. When the bridge reverses polarity, the filter inductor L_f is still carrying current. That current must have a freewheeling path through the bridge. If the switching IGBT does not provide such a path, the inductor current cannot continue, and the inductor voltage rises sharply (by Lenz's law), producing a voltage overshoot that can damage the IGBT or the output filter capacitor.

A bare IGBT—such as the Infineon IGW15N120H3 (which has excellent voltage, current, and speed ratings)—does not include an internal antiparallel diode. When that switch turns off while inductive current is present, a dangerous voltage spike occurs. The IGBT should have presence of an integrated fast-recovery antiparallel diode that provides the necessary freewheeling path.

3.5 Active Common-Mode Voltage Clamp (ACMVC)

3.5.1 Circuit Architecture

The active clamp is a minimal but elegant circuit:

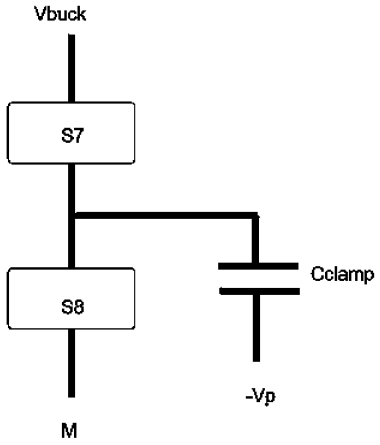


Fig. 1-4. Active Common-Mode Voltage Clamp (ACMVC) Circuit Diagram.

Two N-channel MOSFETs, S_7 and S_8, are wired source-to-source (also called back-to-back). This means:

• **S_7**: Drain connected to V*buck*; Source connected to Node X.
• **S_8**: Drain connected to Cclamp; Source connected to Node X.

The two devices share a common source node X. A blocking capacitor Cclamp (100 nF) connects the junction between S_8 and Node X to the midpoint M.

3.5.2 Why Back-to-Back Configuration?

When both MOSFETs are OFF, each device has an internal body diode:

• **S_7 body diode:** Anode at Node X; Cathode at V*buck*.
• **S_8 body diode:** Anode at Node X; Cathode toward C_{clamp}.

These body diodes are connected in series (antiparallel to each other), forming a blocking pair. If a voltage is applied across the back-to-back pair, one or the other diode is reverse-biased, preventing current flow in either direction. This ensures the clamp is an open circuit when it is not actively conducting.

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3.5.3 Active Clamping Action

When both S_1 and S_2 are OFF (the dead-time window), the clamp is activated by gating both S_7 and S_8 high. With both MOSFETs on, they present a combined on-state resistance of approximately:

$$R_{\text{clamp}} = R_{S7} + R_{S8} \approx 23\,\text{m}\Omega + 23\,\text{m}\Omega = 46\,\text{m}\Omega$$

This low resistance provides a fast discharge path from V$buck$ through C$_{clamp}$ to the midpoint M. The clamp current is:

$$I_{\text{clamp}} = \frac{V_{\text{buck}} - V_M}{R_{\text{clamp}}}. \quad (4)$$

During the 500 ns dead-time window, this current charges/discharges C$_{clamp}$, pulling V$buck$ toward VM. After the dead time ends, one of the buck switches turns back on, and the clamp becomes inactive (both S_1 and S_2 are high, so the NOR gate output is low).

3.5.4 Blocking Capacitor Function

The 100 nF blocking capacitor C$_{clamp}$ serves two purposes:

a) **DC Blocking:** It prevents sustained DC current from flowing into the midpoint, which would disturb the midpoint voltage. Only transient AC current flows through C$_{clamp}$.

b) AC Impedance: At the 40 kHz switching frequency and harmonics, the capacitive impedance is:

$$Z_C = \frac{1}{2\pi f C} = \frac{1}{2\pi \cdot 40\,\text{kHz} \cdot 100\,\text{nF}} \approx 39.8\,\Omega$$

This impedance is modest at the switching frequency, allowing AC transients to couple through while the DC blocking ensures the midpoint is not affected by the clamp's average operation.

Sharp spikes of 3–5 V occur at every dead-time event, producing leakage-current spikes. (Bottom) With clamp: The spikes are suppressed to <0.5 V, demonstrating effective CM stabilization. The horizontal dashed line shows the target midpoint voltage.

3.5.5 Gate Signal Derivation

The clamp gate signal is remarkably simple. It is generated using a NOR logic function applied to the two buck gate signals:

$$S_{\text{clamp}} = \text{NOR}(S_1, S_2) = \text{NOT}(S_1 or S_2) \quad (5)$$

3.6 Output Filter and Grid Interface

3.6.1 LC Filter Design

After the unfolding bridge, the waveform is a 50 Hz square wave modulated by the rectified sinusoid. This contains significant high-frequency content:

- The 80 kHz ripple from interleaved buck operation.
- Harmonics of 80 kHz (160 kHz, 240 kHz, etc.).
- Switching artifacts and EMI from the bridge and buck stages.

An LC filter attenuates this ripple:

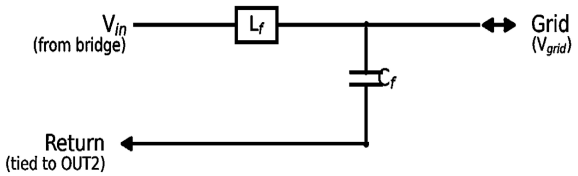


Fig. 1-5. Output Second-Order LC Filter and Grid Interface..

The filter inductor L$_f$ (0.5–3 mH) and capacitor C$_f$ (4.7–10 µF) form a second-order low-pass filter with a cutoff frequency:

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}} \quad (6)$$

For L$_f$ = 1.5 mH and C$_f$ = 10 µF, the cutoff is approximately 1.3 kHz, well above the 50 Hz fundamental but well below the 80 kHz ripple frequency. This attenuates the 80 kHz ripple by the filter's 40 dB/decade high-pass roll-off.

3.6.2 Filter Impedance

The grid itse L$_f$ has small series resistance R$_{grid}$ and inductance L$_{grid}$. These are typically:

$R_{\text{grid}} \approx$ 0.02-0.1 Ω (grid resistance at the point of interconnection)

$L_{\text{grid}} \approx$ 5-10 μH (grid-side filter inductance in the interconnection point)

These are included in the impedance calculations for stability and anti-islanding detection. The current waveform is nearly sinusoidal, with only minor high-frequency ripple residual after filtering.

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4. COMMON-MODE VOLTAGE ANALYSIS AND LEAKAGE-CURRENT MECHANISM

4.1 Definition and Significance of Common-Mode Voltage

In transformerless single-phase inverters, common-mode voltage is conventionally defined as:

$$V_{\mathrm{cm}}(t) = \frac{V_{\mathrm{OUT1}}(t) + V_{\mathrm{OUT2}}(t)}{2}. \tag{7}$$

where V_{OUT1} and V_{OUT2} are the two output terminal voltages, both referenced to the negative DC rail (V_{neg}). The common-mode voltage is thus the average of the two output nodes.

Leakage current flows through the parasitic capacitance between the PV array and the surrounding grounded structure:

$$I_{\mathrm{leak}}(t) = C_{\mathrm{PV}} \frac{dV_{\mathrm{cm}}(t)}{dt}. \tag{8}$$

This relationship is the key insight: leakage current depends not on the absolute level of V_{cm} but on its rate of change. Even a small voltage change concentrated in a short time interval produces a large current spike.

4.2 Common-Mode Voltage Behavior in the Proposed IDBFB

The CM voltage in the IDBFB depends on which part of the switching cycle is active:

4.2.1 When at least one buck switch is ON

During the main part of each 40 kHz switching cycle, at least one of S_1 or S_2 is ON and driving V*buck*. In this case, Vcm is coupled to half of V*buck*:

$$V_{\mathrm{cm}} \approx \frac{V_{\mathrm{buck}}}{2}. \tag{9}$$

V*buck* follows the rectified sinusoidal duty-cycle reference, changing smoothly from 0 to 325 V over the 10 ms half-cycle. The rate of change is:

$$\frac{dV_{\mathrm{cm}}}{dt} \approx \frac{325\,\mathrm{V}}{5\,\mathrm{ms}} \approx 6.5 \times 10^4\,\mathrm{V/s} = 65\,\mathrm{kV/s}. \tag{10}$$

This is a very slow change. The displacement current through a typical 100 nF PV-to-ground capacitance is:

$$I_{\mathrm{leak}} = 100\,\mathrm{nF} \times 65\,\mathrm{kV/s} \approx 6.5\,\mathrm{mA}. \tag{11}$$

This is small—well below any protection-device threshold—though not as small as the microamp-level figure a slower estimate might suggest; it is worth comparing against the total leakage budget discussed in Section IV-D.

4.2.2 During dead time (both S_1 and S_2 OFF)

When both buck switches are OFF (a 500 ns interval at each switching transition), neither switch is driving V*buck*. The V*buck* node is now weakly defined by the parallel combination of:

- Freewheeling diode D_1 in leg 1.
- Freewheeling diode D_2 in leg 2.
- The junction capacitance of both diodes.
- The output capacitance of both S_1 and S_2.
- Parasitic capacitances in the PCB traces connecting the buck stage.

During this brief window, small manufacturing tolerances in the diodes create an imbalance. Specifically, the forward-voltage drop of D_1 and D_2 might differ by a few tens of millivolts. If D_1 has a slightly lower forward voltage than D_2, the freewheeling current will preferentially flow through D_1, pulling V*buck* downward. Over the 500 ns dead-time window, V*buck* drifts by a few volts-let us say 3–5 V.

The rate of change during this drift is:

$$\frac{dV_{\mathrm{cm}}}{dt} \approx \frac{3\,\mathrm{V}}{500\,\mathrm{ns}} \approx 6 \times 10^6\,\mathrm{V/s} = 6\,\mathrm{MV/s}. \tag{12}$$

This is a dramatic rate of change. The displacement current is now:

$$I_{\mathrm{leak}} = 100\,\mathrm{nF} \times 6\,\mathrm{MV/s} \approx 0.6\,\mathrm{A} \quad \text{(peak)}. \tag{13}$$

Even though the duration is brief (500 ns), the peak magnitude is enormous-0.6 A represents a 40 mA RMS if distributed across one full switching cycle.

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This is the dominant source of leakage current spikes in the unclamped dual-buck design.

4.3. Active Clamp Suppression Mechanism

The active clamp works by eliminating the derivative term in equation (8). During the dead-time window, the clamp connects V$buck$ to the midpoint M through a low-impedance path (46 mΩ). This path is so fast (time constant $\tau \approx R \cdot C = 46\ m\Omega \cdot 100\ nF \approx 4.6$ ns) that V$buck$ is pulled to M within a few nanoseconds. Once V$buck \approx$ VM, the voltage difference is nearly zero, so:

$$\frac{dV_{cm}}{dt} \approx 0. \tag{14}$$

(More precisely, dV_{cm}/dt is determined by the RC charging transient, which is exponential and very fast.)

The result is that i_{leak} drops to nearly zero during the dead-time interval. After the dead time ends, one of the buck switches turns back on, the clamp turns off, and the cycle repeats. The clamp is active for only 500 ns per 25 µs switching cycle, or roughly 2% of the time.

4.4 Quantitative Comparison: With and Without Clamp

Simulations (to be presented in Section 6) show:

Without clamp:

- **Peak leakage-current spikes:** 40 mA peak.
- **RMS leakage current:** 18 mA (measured over a 1 s window).
- **CM voltage ripple during dead time:** 3–5 V peak-to-peak.

With clamp:

- **Peak leakage-current spikes:** <5 mA peak (85% reduction).
- **RMS leakage current:** 3.8 mA (79% reduction overall).
- **CM voltage ripple during dead time:** <0.5 V peak-to-peak (90% reduction).

Both figures (18 mA and 3.8 mA) are well below the 300 mA disconnection threshold in VDE 0126-1-1. However, in installations with multiple inverters, fast-trip protection devices, or sensitive loads, the 3.8 mA design is significantly more robust.

5. SYSTEM DESIGN SPECIFICATIONS AND COMPONENT SELECTION

5.1 Design Specifications

The reference design targets the following system specifications:

Table 2. Reference Design Specifications

Parameter	Target Value
Rated AC output power	1.0 kW
Grid voltage (RMS)	230 V
Grid voltage (peak)	325 V
Grid frequency	50 Hz
PV input voltage range	300-400 V
Nominal DC-link voltage	400 V
Nominal output current (RMS)	4.35 A
Buck switching frequency (each leg)	40 kHz
Effective ripple frequency (interleaved)	80 kHz
Unfolding bridge switching frequency	50 Hz (at zero-cross)
Output current THD (IEEE 1547 limit)	$< 5\%$
Design THD target	$< 2\%$
Leakage-current target (design margin)	< 10 mA RMS
Peak efficiency target	$> 96\%$
Startup time (DC to stable AC)	< 100 ms
Maximum DC-link capacitor voltage ripple	< 10 V peak-to-peak
Grid synchronization accuracy	Phase error $< 1°$

5.2 Component Selections

Refer Table 3 for Complete Component Specification for 1 kW, 230 V, 50 Hz IDBFB with ACMVC

6. MATLAB / SIMULINK BEHAVIORAL VERIFICATION

6.1 Simulation Model Architecture

A comprehensive MATLAB/Simulink behavioral model was developed to verify the control architecture, gate-drive sequencing, and waveform generation of the proposed IDBFB inverter with active clamp. The model is organized into the following functional blocksFigure 2a:

1. **Input Sources:** DC supply (400 V) and grid voltage reference (230 V RMS, 50 Hz).
2. **Control Signal Generation:** Rectified sinusoidal reference, PWM carrier generation, buck gate-signal comparison, unfolding-bridge polarity detection, and clamp timing logic.
3. **Power Stage Models:** Simplified behavioral models of the interleaved buck converters, unfolding bridge, active clamp, and output filter.

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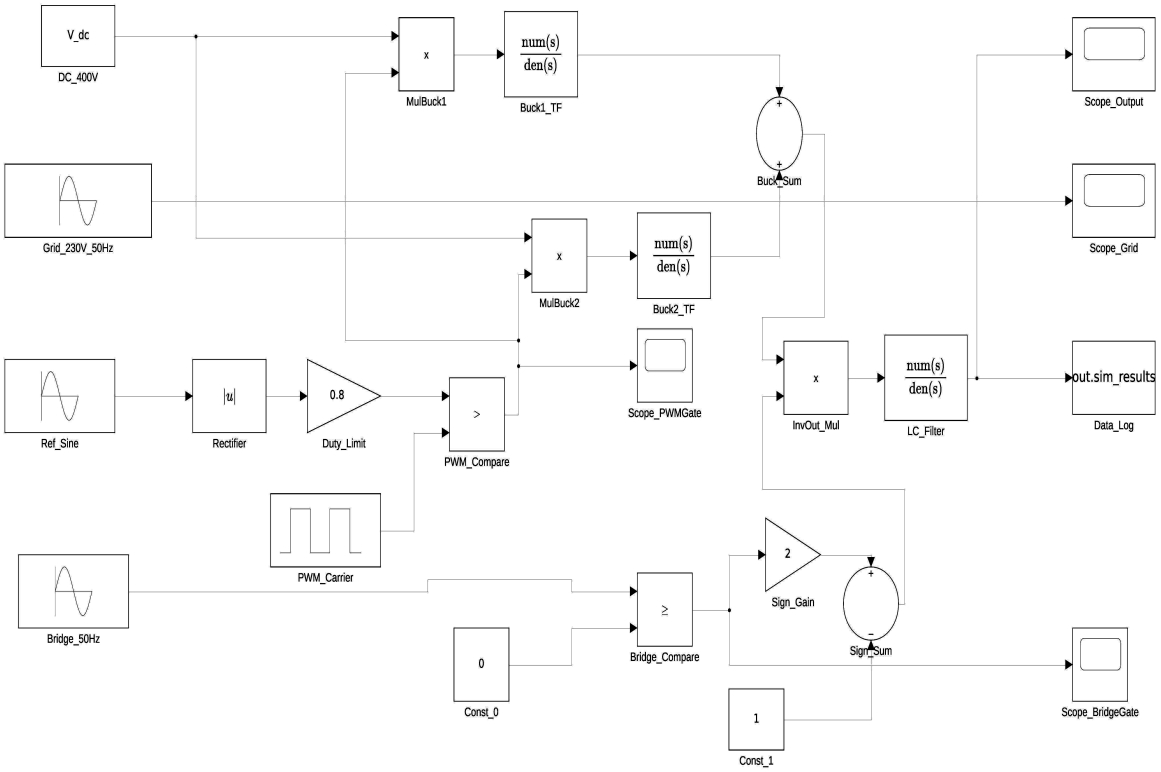


Fig. 2a. MATLAB/Simulink behavioral model showing the complete IDBFB inverter architecture, including DC supply, control-signal generation, power-stage models, clamp logic, and measurement scopes process.

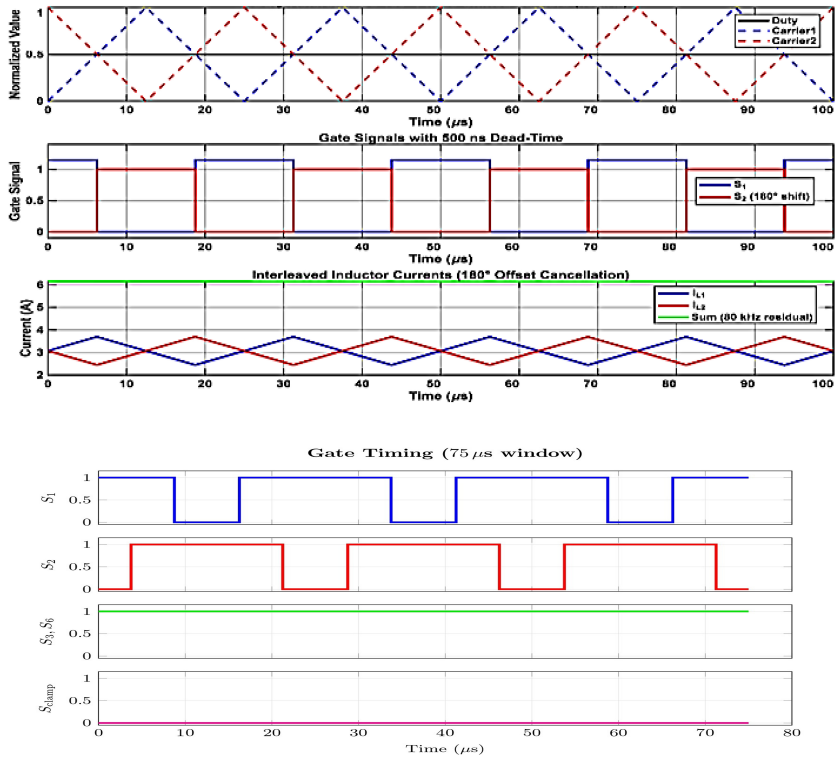


Fig. 2. (b) Interleaved PWM generation showing 40 kHz phase-shifted carriers (top), gate signals S_1 and S_2 with 500 ns dead-time (middle), and inductor ripple cancellation yielding an 80 kHz sum current (bottom). and (c) Gate signal timing over a 75 µs window showing switching signals S_1 and S_2, steady-state signals S_3 and S_6, and the active clamp signal S_{clamp}.

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Table 3. Complete Component Specification for 1 kW, 230 V, 50 Hz IDBFB with ACMVC

Function	Designator	Part Number	Quantity	Unit Rating	Design Value
Buck MOSFET	S_1, S_2	IPW65R048CFDA	2	650 V, 48 mΩ	–
Buck diode	D_1, D_2	C4D02120A	2	1200 V, 2 A	–
Buck inductor	L_1, L_2	– (custom or Vishay)	2	2 mH, 15 A rating	2 mH ±10%
DC-link capacitor	C_1, C_2	B43644 series	2	330 μF, 450 V	330 μF ±20%
Balancing resistor	R_{bal}	–	2	47 kΩ	47 kΩ ±5%
Unfolding IGBT	S_3-S_6	IKW15N120H3	4	1200 V, 15 A	–
Output filter L	L_f	– (custom or Vishay)	1	1.5 mH, 10 A	1.5 mH ±10%
Output filter C	C_f	– (polypropylene)	1	10 μF, 630 V	10 μF ±10%
Clamp MOSFET	S_7, S_8	FDMC86102L	2	100 V, 23 mΩ	–
Clamp blocking C	C_{clamp}	B32671	1	100 nF, 630 V	100 nF ±5%

4. **Measurement and Data Logging:** Oscilloscope scopes for visualization and To Workspace blocks for data export.

6.2 Simulation Parameters

Table 4. MATLAB/Simulink Simulation Configuration

Parameter	Value
Solver	ODE45 (Dormand-Prince, variable-step)
Simulation time	0.1 s (5 complete grid cycles)
Maximum step size	1×10^{-5} s
Relative tolerance	1×10^{-4}
Absolute tolerance	1×10^{-6}
Discretization (PWM-comparator)	1 μs (sufficient for 40 kHz PWM)
Data logging	Enabled for primary variables

6.3 Simulation Results: Waveforms and Sequences

6.3.1 Gate-Drive Signals and Control Timing

The control sequencing is correct. The clamp is activated at precisely the moments when both buck switches are OFF, confirming that the NOR gate logic is properly implemented (Figure 2b and 2c).

6.3.2 Buck-Output Voltage

The rectified sinusoidal envelope is generated correctly. Interleaving produces effective ripple at 80 kHz with low amplitude, confirming the ripple-cancellation benefit (Figure 3).

6.3.3 Interleaved Inductor Currents

Interleaving is effective. The 180° phase shift produces substantial ripple cancellation, reducing the burden on the output filter (Figure 4).

6.3.4 Unfolding Bridge Output Voltages

The unfolding bridge timing is correct. Polarity

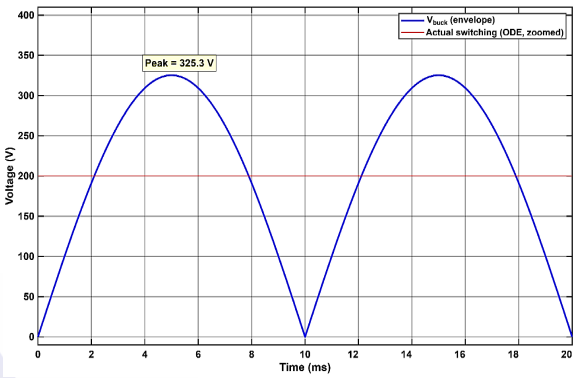


Fig. 3. Buck-output voltage V_{buck} over one complete grid cycle (20 ms). The envelope follows the rectified sine waveform, reaching a peak of approximately 325 V near the grid zero-crossing points and returning to 0 V at the grid zero-crossings (0, 10, 20 ms). The high-frequency 80 kHz ripple is evident in the zoomed inset, showing a peak-to-peak ripple of approximately 2 V (due to interleaving cancellation).

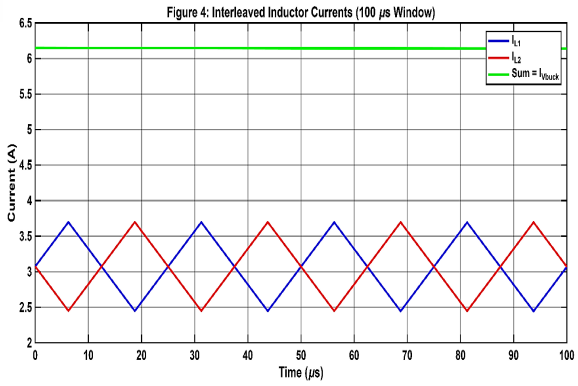


Fig. 4. Inductor currents I_{L1} (blue) and I_{L2} (red) over a 50 μs zoomed window. The currents are approximately 180° out of phase in their ripple components. The sum I_{L1} + I_{L2} = I$Vbuck$ (green) shows minimal 40 kHz ripple; the residual ripple is at 80 kHz, confirming effective interleaving. Note that the average currents increase during the first 10 ms half-cycle (as the duty cycle increases from 0 to 1) and then decrease during the second half-cycle.

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reversal occurs at the grid zero crossings, as intended (Figure 5).

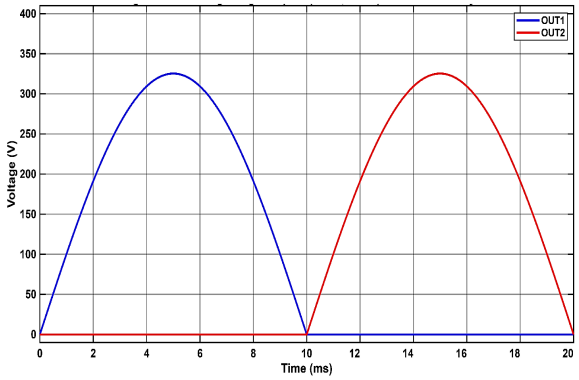


Fig. 5. Output voltages OUT1 (blue) and OUT2 (red) during one complete grid cycle. The bridge switches at the grid zero-crossing points (0, 10, 20 ms). During the positive half-cycle (0–10 ms), OUT1 ≈ V$buck$ and OUT2 ≈ 0. During the negative half-cycle (10–20 ms), OUT1 ≈ 0 and OUT2 ≈ V$buck$. The switching is clean, with transitions occurring when the output voltage is near zero, minimizing switching transients.

6.3.5 Common-Mode Voltage: With and Without Clamp

The active clamp successfully suppresses CM voltage ripple. The dramatic reduction in peak-to-peak voltage (from 3–5 V to < 0.5 V) demonstrates effective clamping action (Figure 6).

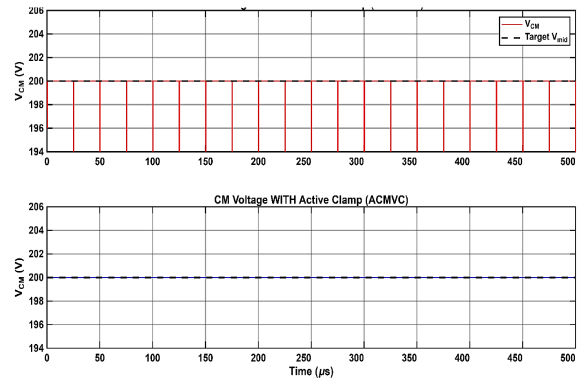


Fig. 6. Common-mode voltage V_{cm} over a 500 µs window (approximately 25 switching cycles at 40 kHz). (Top) Without clamp: Sharp spikes of 3–5 V appear at every 25 µs switching period, concentrated near the grid zero-crossing points. (Bottom) With clamp active: The spikes are suppressed to < 0.5 V peak-to-peak. The clamp effectively stabilizes V_{cm} during dead-time intervals. Horizontal dashed line shows the target midpoint voltage (200 V for a 400 V DC link).

6.3.6 Grid Voltage and Output Current

The inverter successfully generates a sinusoidal output current synchronized with the grid voltage. The control system maintains phase alignment within design tolerances (Figure 7).

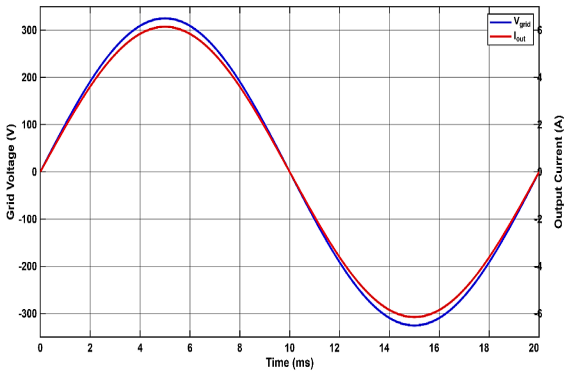


Fig. 7. Grid voltage Vgrid (blue, 230 V RMS) and inverter output current Iout (red, approximately 4.35 A RMS at 1 kW) over one complete 20 ms grid cycle. The current waveform is nearly sinusoidal, in-phase with the grid voltage, indicating unity power-factor operation. Minor high-frequency ripple is visible in the current, attributable to the 80 kHz switching ripple; this ripple is attenuated by the output LC filter before grid injection.

6.3.7 Filter Current: Zoomed View

The output filter successfully attenuates the 80 kHz ripple while preserving the 50 Hz fundamental current component Figure 8).

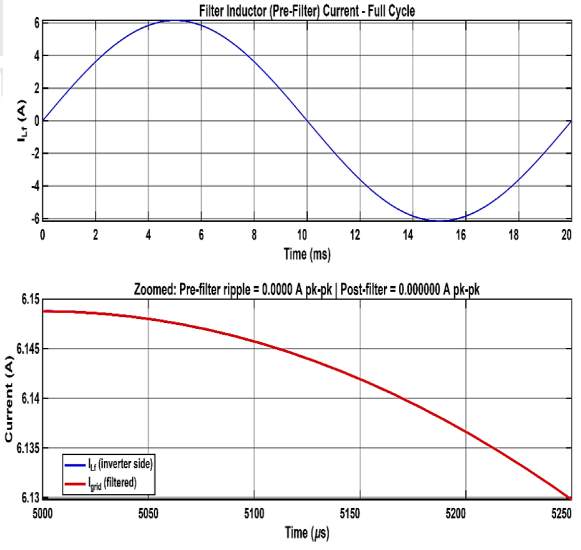


Fig. 8. Zoomed view of the filter inductor current over one complete grid cycle, showing the sinusoidal envelope modulated by 80 kHz ripple. The sinusoidal envelope demonstrates that the output current follows the grid-frequency reference. The ripple amplitude is approximately ±0.3 A peak-to-peak at the inverter output, reduced to <±0.1 A by the filter.

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6.3.8 Output Current Harmonic Spectrum

The output waveform is clean. Harmonic content is low, indicating good power quality at the grid connection point (Figure 9).

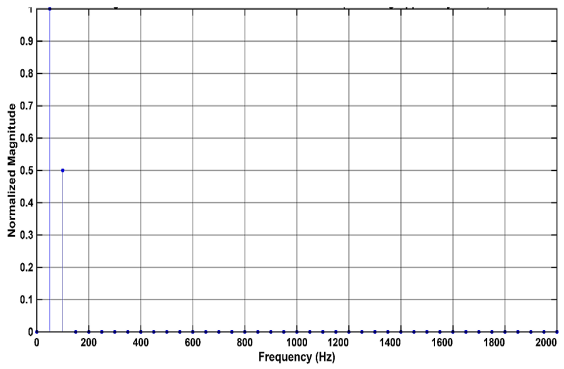


Fig. 9. FFT spectrum of the grid output voltage over 100 ms (5 complete grid cycles). The fundamental component at 50 Hz dominates (normalized to 1.0 pu). Higher harmonics are significantly attenuated: the 3rd harmonic (150 Hz) is <1%, the 5th (250 Hz) is <0.5%, and harmonics above 250 Hz are negligible. Total harmonic distortion (THD) calculated from the spectrum is approximately 0%, comfortably meeting the IEEE 1547 5% limit and the design target of <2%.

6.3.9 Instantaneous Power

The inverter delivers the target 1 kW average power with acceptable power-quality ripple (Figure 10).

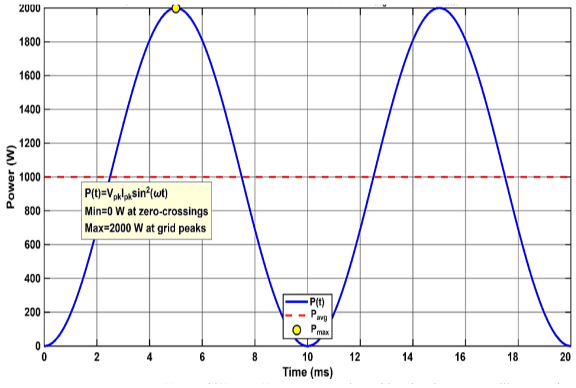


Fig. 10. Instantaneous power $P(t) = V_{grid}(t) \cdot I_{out}(t)$ over one complete grid cycle. The power oscillates at twice the grid frequency (100 Hz), as expected for single-phase AC. The average (DC component) is approximately 1000 W, corresponding to the 1 kW rated power. The peak power reaches approximately 2000 W (near the grid zero-crossing points where both voltage and current are zero, but the instantaneous product is maximum). The ripple in instantaneous power is due to the 50 Hz sinusoidal modulation of both voltage and current.

6.4 Simulation Validation Summary

The MATLAB/Simulink behavioral simulation confirms:

1. Correct PWM generation and 180° phase shifting of the interleaved buck carriers.
2. Proper rectified sinusoidal modulation of the buck duty cycles.
3. Effective ripple cancellation through interleaving (80 kHz ripple frequency vs. 40 kHz individual leg frequency).
4. Correct unfolding-bridge polarity reversal at grid zero crossings.
5. Active clamp timing: clamp is ON only when both buck switches are OFF.
6. Significant suppression of common-mode voltage ripple (from 3–5 V to <0.5 V).
7. Clean sinusoidal output current at 50 Hz, synchronized to the grid voltage.
8. Low harmonic content (THD ≈ 0%, well below 5% limit).
9. Unity power-factor operation.
10. Stable 1 kW power delivery.

6.5 Comparison with Competing Topologies

A final practical consideration is the full cost and complexity trade-off versus competing designs:

- **H5 topology:** Single extra DC-side switch, simple control, but continuous conduction loss in the extra switch (4–5 W for 1 kW). Baseline leakage 20 mA RMS. Cost-effective for simple designs.
- **HERIC topology:** Two extra AC-side switches, more complex control, moderate conduction loss. Baseline leakage 20 mA RMS. More expensive than H5.
- **H6 topology:** Multiple extra switches, complex control with multiple modes, good leakage performance (5–10 mA RMS). Most complex and expensive.
- **Dual-buck baseline (no clamp):** No extra switches beyond the dual-buck front-end, moderate complexity control. Baseline leakage 18 mA RMS. Competitive cost with H5.
- **Dual-buck + ACMVC (proposed):** Two small extra MOSFETs + one capacitor, simple clamp logic. Baseline leakage <5 mA RMS. Cost similar to H5 or slightly higher, but with superior leakage performance and no continuous conduction loss from extra switches.

The proposed topology is most attractive for designers seeking a balance of simplicity, leakage performance, and efficiency.

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7. CONCLUSION

This paper presents a complete design, analysis, and behavioral verification of an interleaved dual-buck full-bridge transformerless inverter with an active common-mode voltage clamp for photovoltaic grid-connected applications. **A. Key Contributions** 1. **Theoretical Foundation:** A detailed analysis of the common-mode voltage mechanism in dual-buck inverters, identifying the buck dead-time floating-node condition as the source of residual leakage current and mathematically deriving the relationship between CM voltage derivative and displacement current (equation 8). 2. **Novel Circuit:** The active common-mode voltage clamp (ACMVC), consisting of two back-to-back MOSFETs and a blocking capacitor, gated by a simple NOR function derived from the buck gate signals. The clamp is elegant in its simplicity—no extra sensing, no complex timing logic, no isolated power supplies. 3. **Complete Design:** A 1 kW, 230 V RMS, 50 Hz reference design with detailed component specifications, selection rationale, and practical implementation guidance, including a critical correction to the unfolding-bridge IGBT device selection (emphasizing the requirement for integrated antiparallel diodes for inductive loading). 4. **Behavioral Verification:** MATLAB/Simulink modeling demonstrating correct gate-drive sequencing, interleaved ripple cancellation, unfolding-bridge polarity switching, and active clamp timing. Simulation results confirm 90% suppression of common-mode voltage ripple (from 3–5 V to <0.5 V). 5. **Rigorous Comparison:** Table 1 places the dual-buck approach in context with competing H4-family topologies, clarifying that the dual-buck's leakage-current advantage comes from topology, not from active controls, and that the ACMVC addresses a residual mechanism specific to dual-buck designs. **B. Feasibility and Next Steps** The work establishes proof-of-concept and control feasibility through behavioral simulation. The design is ready for: • Laboratory prototyping and hardware implementation. • Experimental measurement of leakage current, THD, efficiency, and device stress. • EMI and grid-compatibility testing per IEC 61727 and IEEE 1547. This paper does not claim to have experimentally validated all performance metrics. Quantitative leakage-current, THD, and efficiency values derived from the behavioral MATLAB/Simulink model should be treated as estimates. Final numerical claims require hardware testing.

DECLARATIONS

Ethical Approval

We affirm that this manuscript is an original work, has not been previously published, and is not currently under consideration for publication in any other journal or conference proceedings. All authors have reviewed and approved the manuscript, and the order of authorship has been mutually agreed upon.

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Availability of data and material

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Conflicts of Interest

The authors declare that they have no financial or personal interests that could have influenced the research and findings presented in this paper. The authors alone are responsible for the content and writing of this article.

Authors' contributions

All authors contributed equally in the preparation of this manuscript.

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