

RESEARCH ARTICLE

Quadruple Gate Spin–FET: A Novel Approach to Power–Efficient Reconfigurable Logic Design Beyond CMOS

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ABSTRACT: This work presents a compact electrical model of a quadruple-gate spin field-effect transistor (QGSFET) for power-efficient and reconfigurable logic beyond conventional CMOS technology. The proposed device exploits independent multi-gate control to realize both two-operand and three-operand logic functions using a common channel length, thereby providing enhanced functional flexibility without requiring separate device geometries for different logic operations. The QGSFET is modeled in Verilog-A and implemented in the Cadence simulation environment, where we systematically evaluate its electrical characteristics and switching behavior through DC and transient analyses across different channel lengths. The proposed multi-gate configuration enables reconfigurable implementations of AND, NAND, OR, NOR, XOR, XNOR, three-input XNOR, Majority Gate, and Complementary Majority Gate functions, demonstrating the versatility of the device for compact logic design. A 1-bit full adder and a 2-bit binary adder are further developed using QGSFET-based logic. Comparative evaluation with conventional CMOS and previously reported Spin-FET-based implementations demonstrates reductions in device count, power consumption, propagation delay, and energy consumption, together with improved area efficiency. The results establish the QGSFET as a promising device architecture for low-power, compact, and reconfigurable nanoscale logic circuits, highlighting its potential for beyond-CMOS computing applications.

Keywords: QGSFET, Spin-FET modeling, Beyond CMOS technology, quadruple Gate Spin-FET, logic gates, multi-gate spin-FET

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1. INTRODUCTION

The majority of applications in the modern world are powered by electrical devices. When building the internal design of electronic circuits, the three crucial VLSI design parameters should be carefully observed viz; area, power, and speed. Moore's law predicts that in the near future, the number of transistors will grow exponentially, resulting in

both higher power dissipation and technological improvements, which will ultimately lead to information loss. We would have concentrated on the transistor count before using the circuits. In combinational and sequential circuits, gates are the basic building blocks of most electronic circuits. While designing the circuit that mitigates the power dissipation factor, we would have given priority to the gate, the number of transistors, and logic style selections [1]. It has been noted that when devices shrink in size, second-order effects become evident, and they enter the nano-regime. These brief channel effects get so intense that they interfere with the devices' operating ability. Regarding technology, it is imperative that devices be further scaled in order to expand functionality, which will undoubtedly take a significant amount of work [2].

In light of this, the researchers have considered a

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number of potential technologies, novel materials, and geometries of spin-FETs [3]. The major research has been carried out on channel material and geometry of spin transistors. However, very less effort has been put into the circuit simulation part and the reconfigurable logic circuit design. One of the most promising novel opportunities for spintronics research is the application of the spin degree of freedom in integrated circuits and active semiconductor devices. While considering the circuit application part, researchers have designed various logic gates using single-gate and multi-gate spin transistors. In [4-7] explain double-gate, triple-gate, and quadruple-gate-based logic circuit applications. This article introduces a quadruple-gate spin field-effect transistor that takes into consideration the reconfigurable spin function of multiple operands [8]. Using spin FETs, we proposed and designed 2-operand and 3-operand spintronic reconfigurable logic gates to reduce channel length compared with previously reported work, along with a full adder and a 2-bit binary adder circuit. We demonstrated that a single QGSFET, rather than many CMOS devices, could implement all symmetric Boolean gates, including AND, OR, XOR, NAND, NOR, XNOR, and the Majority Gate. With significantly fewer devices than traditional CMOS, we also used QGSFETs to develop the structure for a 1-bit full adder and a 2-bit binary adder. Also, the ability of QGSFETs to implement all six 2-input logic gates at a single fixed channel length ($L = 600$ nm) and 3-input gates at two lengths, drastically cutting adder device counts. These circuits consist of nonvolatile functionalities that can be altered by varying the spin transistor's magnetization configurations. The potential application of

the spin degree of freedom in active devices concept has been explored. In this study, we modeled the mathematical equation using Verilog A language and proposed a new reconfigurable logic design for 2-operands and 3-operand logic gates. A 1-bit full adder and a 2-bit binary parallel adder may realize digital input without a floating gate due to QGSFET. Reconfigurable logic gates represent a paradigm shift in digital circuit design, offering greater flexibility, adaptability, and potential for innovation compared to traditional, fixed-function logic gates [8, 9].

Figure 1 depicts the spin transistor structure for local geometry. The electrical model of the spin transistor has been designed employing the Verilog A language with a Cadence platform [10]. The Datta-Das [11] theory has been used to model this device. However, configurable logic was developed using multiple spin transistor gate structures [12].

In this research, the reconfigurable electrical model has been developed for a quadruple-gate spin-FET to study the functionality of digital circuits for two operands, three operands, and adder circuits, which can be utilized for the digital logic design. Reconfigurable QGSFET for 3-input and 2-input functions was modeled using the Computer-Assisted Design (CAD) tool. Based on the Datta-Das theory [13] spin-FET channels were optimized based on the type of material used in the channel region. The DC analysis shows that the channel length variation changes output voltage. However, the transient analysis proves the function works digitally at GHz frequency. The parameters taken for the simulation are based on calibrated models and verified by established literature [14-17].

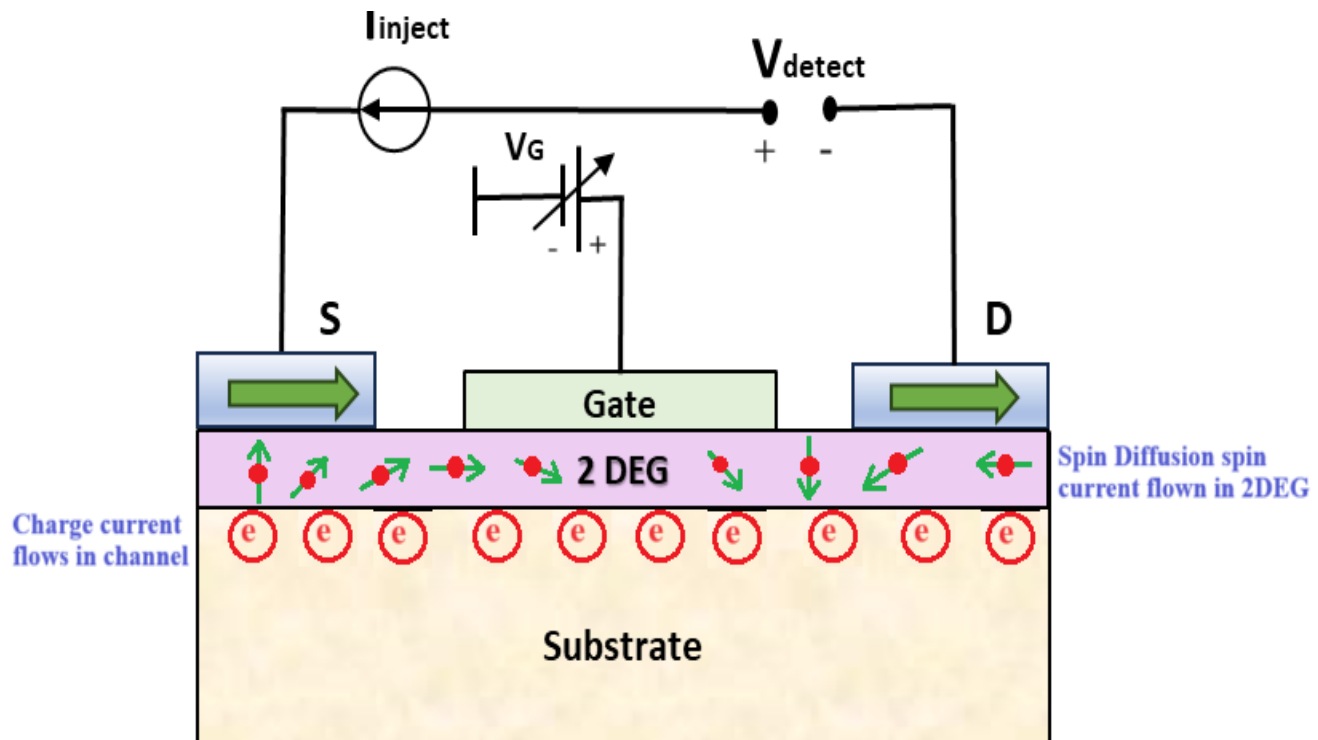


Fig. 1. The Structure of the Datta- Das Transistor [10].

Numerous spin-based logic structures, including memory and the complete adder, have been proposed by [18-20]. Using a quadruple spin-FET, we designed spin-based logic gates viz. AND, NOR, XOR, OR, XNOR, NAND, full adder, 2-bit binary adder, and the transient simulation validates their logic functionality. The power analysis and transit time section also discusses the device's operation speed and power consumption based on the simulation results. The research work has been structured as follows: Device modeling of Quadruple gate Spin Transistor is explained in Section 2. The concept of reconfigurability using QGSFET for 3-input and 2-input functions has been described in Section 3. The transient time and power analysis of spin-based digital gates is also discussed in this section. Section 4 explains the potential fabrication challenges in QGSFET, where the paper has summaries in Section 5.

2. DEVICE MODELING AND SIMULATION

Spin-FETs and Spin-MOSFETs are promising devices that introduce nonvolatility by orienting the ferromagnetic source and drain relative to each other. Despite several fundamental challenges, including spin injection from metals to ferromagnets and from ferromagnets to semiconductors, as well as issues related to spin propagation, relaxation, and manipulation via gate voltage, these devices are advantageous over CMOS. Viktor Sverdlov et al. [21] demonstrate the concepts of logic-in-memory and in-memory computing architectures utilizing Spin-FET technology. This advancement paves the way for a novel computing paradigm characterized by low power consumption and high performance, wherein information processing and storage occur within the same nonvolatile components.

The Gefei Wang et.al. [4], has proposed a novel device called double-gate spin-FET. They develop an electrical model for double-gate spin-FET. The electron spin property is used for the modulation of multi-gate voltages sequentially. The DC simulation validates the functionality of the double-gate electrical model for performing different logical operations. Viz. Full adder, XOR gates, and NAND gates. The author Gul Faroz Malik et.al. [5] has developed triple gate spin-FET for low power consumption and faster switching speed. They implemented 3-input XOR, 3-input XNOR, and majority gate functions using the modeled TGSE.

We proposed a Four-gate spin transistor using reconfigurable logic-based devices with nonvolatility and reduction in power consumption. However, most studies rely on basic Datta-Das transistor models without reconfigurable multi-operand logic. The QGSFET provides better reconfigurability and power efficiency while considering the existing spin-FET model (double-gate and triple-gate). Moreover, this work extends to four gates which allow more complex logic reconfiguration in a single device. The Verilog A modeling captures multi-input functionalities better. The device key parameters have been explicitly explored while considering CMOS and previously reported spin-FET in

terms of power dissipation, speed, and channel length. Unlike traditional transistors, which store information using charge, a Spin-FET uses the magnetic states of ferromagnetic materials to encode logic values. The magnetization states are stable and do not require periodic refreshing, unlike charge-based DRAM, which leaks charge over time. The "Quadruple" nature refers to the ability of the Spin-FET to have four distinct resistance states instead of the usual binary states in conventional transistors. These states are achieved using spin polarization and magnetization alignment, which result in different levels of current flow. The Spin-FET utilizes Spin-Orbit Torque (SOT) or Spin Transfer Torque (STT) to switch between states. Once a state is set, it remains stable without the need for continuous power, reducing energy consumption drastically. Since information is stored magnetically rather than electrically, there's no leakage current.

This removes the need for refresh cycles, as required in conventional volatile memory (like DRAM), leading to significant energy savings. The ability to retain data without power makes Spin-FET-based devices ideal for low-power applications and instant-on computing. Multiple configurations, including Double-Gate and Triple-Gate SFETs, have been reported using the spin-FETs. These models can be used to create different logic circuits and evaluate their performance in [19, 22, 23]. The selection of the gate was primarily objective to demonstrate the variety of logic function implementations provided by the QGSFET. The Datta-Das FET, also referred to as a hybrid spin-FET, where a non-ferromagnetic channel is placed between the two ferromagnetic channels [11]. When the electrons change their states from spin up or spin down, it affects the spin degree of the electron. Spin is the pseudo-vector that has magnitude and direction. Using spin degree of freedom has several benefits, including the ability to encode the two bits, 0 and 1, by making an electron's polarization bistable when it is exposed to a magnetic field. Thus, by flipping the spin, the device can transition between bits and reduce power dissipation [24]. Very few researchers have reported their work in the open literature on circuit design or the application part of the spin-FETs. H. C. Koo et al. [21] created a spin-based ring oscillator, NOT gate and AND gate. Also, Wang G. et al. [27] have reported their work by using a spin-transistor and designing a spin-based NOR gate and AND logic gate using a spin-based inverter and CMOS transmission gate for 1200 nm channel length. The designing of the NAND and XOR gates has also been implemented through multi-gate spin transistors [6]. In [27, 28], basic logic gates have been designed using the single-gate spin-FET. Using a multi-gate spin transistor, the author [7] designed 3-input logic functions. With the multi-gate concept in mind, we designed the QGSFET circuit and modeled this device to carry out a variety of logical functions. Figure 2 depicts the QGSFET's schematic device construction. Here, we set the electrodes' magnetization directions and kept them parallel to one another, the direction can be reversed, and many logical circuit actions have been observed. The Rashba effect occurs at the 2-DEG channel region, and the orientation of the spin

electron has been controlled through gate voltage applied at the transistor. The channel uses the 2DEG material for the highest spin-orbit interaction. Tunneling resistances R_{1-P} and R_{2-P} are modest when the direction of magnetization is parallel (P) to that of the source and drain electrodes; consequently, the output current (drain current) is high. However, when the source electrode and drain have antiparallel (AP) magnetization, the tunneling resistances R_{1-AP} and R_{2-AP} are high, resulting in a low output current [10]. By connecting the numerous input gate electrodes to the

single Quadruple Spin-FET without the use of a floating gate, it is possible to sum the multiple input signals. This is made possible by the fact that the material utilized in the channel and the total quantity of electrons in the 2-DEG channel affect the electrical properties of the Spin-FET. The device has an advantage over conventional CMOS because of its fast-switching speed, non-volatility, and low power consumption. However, the tunneling nature of the drain current (I_D) and source current (I_S) is the source of its high magneto-current ratio.

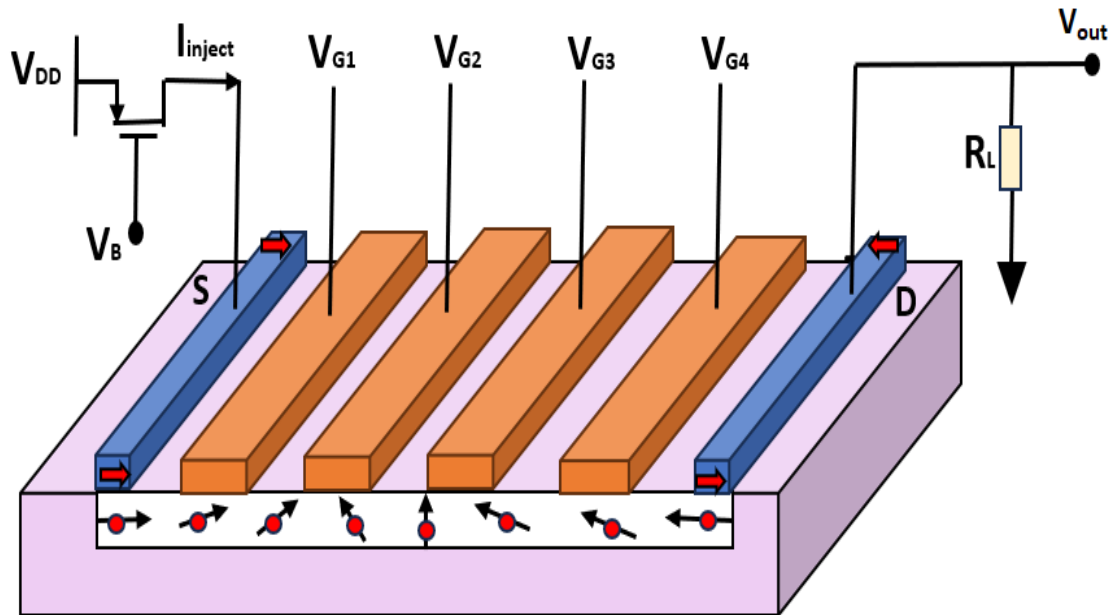


Fig. 2. Structure of QGSFET Spin-FET

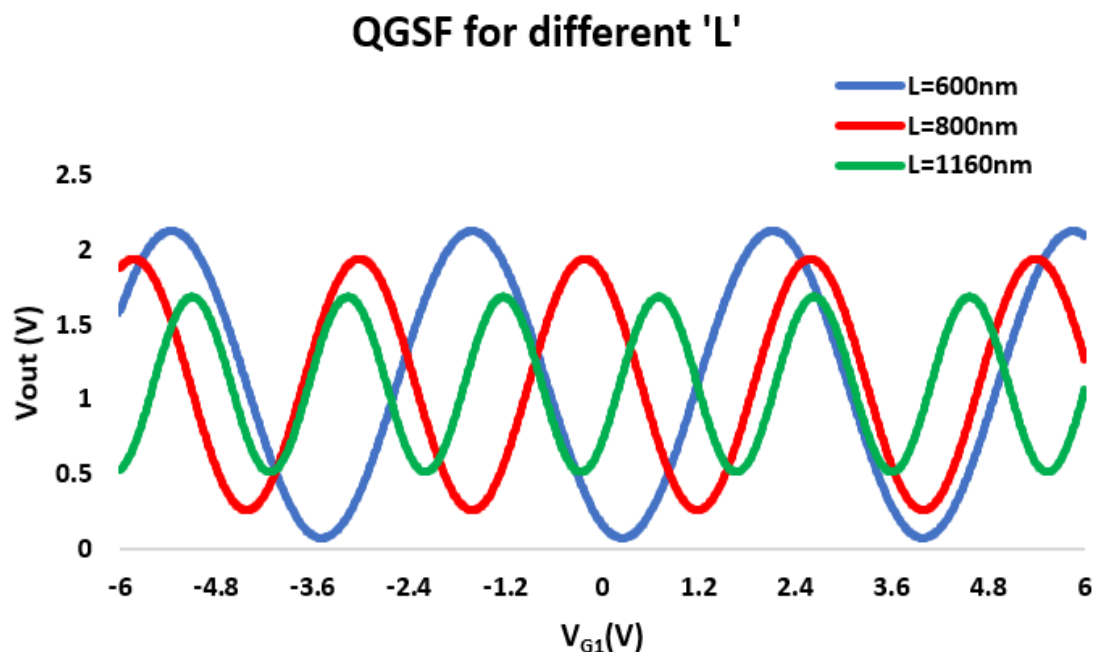


Fig. 3. DC Analysis of QGSFET for different Channel Lengths.

2.1. DC Analysis for QGSFET

The theory of Datta-Das [13, 15] has been designed to perform static simulations for current and voltages. With the help of DC analysis, by selecting different channel lengths and channel resistance, we get maximum and minimum output voltage when $V_G = 0$ V and $V_G = 1.2$ V, respectively, for $L = 800$ nm, which is suitable for performing logical circuit analysis for QGSFET. However, for different channel lengths, we observe maximum and minimum output voltage for different values of V_G . Figure 3 shows the output voltage for different channel lengths [29]. The output's reliance on the channel length is demonstrated by the DC simulation. However, different channel lengths give optimal output voltage to perform logic circuits.

The truth table creation to achieve distinct logic functions for different channel lengths with varying ON and OFF voltages is indicated by the output peaks and valleys changing with the provided input voltage values. It can perform different logical functions with the help of a one-controlling terminal or two controlling inputs. The second function, spin control, is carried out by the channel when it is subjected to the electric field through a gate. The source side is polarized by ferromagnetic material, and the carriers' spin becomes polarized as soon as they pass through the source channel interface. The carrier's spin is not optimally impacted as it continues to move across the NFM (non-ferromagnetic) channel, and the 2DEG is created on the channel surface.

Analogously, the voltage at the third terminal is adjusted between 0 V to 5 V for two operands and between 0 V and 1 V for three operands. Figure 5 illustrates how varying voltages at the control terminal alter the peak and valley points for various output signals. Several logic functions have been obtained through the same gate by taking advantage of this characteristic. It ought to be mentioned that the reconfigurability capability has only been demonstrated with distinct integer control voltages. Nonetheless, the devices can perform a variety of tasks at various fractional control voltages. Tables 3 and 4 provide the values of the parameters that were used to design different logical functions. In order for the spin precession angle to be odd or even multiples of the gate voltage in an electrical application, the channel length needs to be properly constructed so that the measured voltage is either higher or lower in the absence of the gate voltage [30]. The detected voltage is also considerably influenced by channel resistance (R_N) and the length of the channel. The different channel length shows the different detected voltages; however, we require a maximum output voltage for digital circuits to work. Therefore, the local geometry shows the maximum detected voltage as compared to the non-local geometry discussed by Wang G. et al. [27]. The cascading operation of a digital circuit requires local geometry. To perform various logical functions with the optimum detected voltage to adjust the channel's lengths and resistance. At a given gate voltage, the spin precession angle in local and nonlocal signals should be the same for the InAs. In InAs, the output voltage gets a maximum at $V_G = 0$ V and a minimum value at $V_G = 1.2$ V for $L = 800$ nm. For another

heterojunction channel, the output voltages are obtained differently for the value of V_G [27]. Also, the vertical structure of InAs in the quantum well is 2 nm, whereas other heterojunctions have 6 nm to 20 nm, which confines the high mobility at the channel region [16]. In the channel region, we get maximum carrier density and mobility of electrons at 2-DEG for InAs. However, the spin relaxation time of electrons is also $1.61 \mu\text{m}$ [16, 24]. The slight gate voltage shift is the only parameter that may be altered for the optimal curves.

The drain electrode's relative magnetization determines whether the transistor will function as a normally ON or normally OFF transistor [6]. The charge current is a current that results from a potential difference caused by the difference in the amount of electrons at the source and drain sides. This charge current must be addressed because it impairs the device's functionality. Using a non-local setup to ground it can help reduce its impact. Figure 1 depicts a single gate spin-FET's construction [15]. The injected current in Figure 1 was obtained using a current source, where the injected current can be controlled to a desired value using the applied V_G . The ferromagnetic source terminal receives this steady current, polarizing it to the appropriate spin. Because of the Rashba Effect, the V_G causes the orientation of the injected spins to rotate by a certain angle. The drain functions like a filter, preferentially transmitting the spin of one polarization while blocking the spin of the opposite polarization. The output voltage (V_{out}) and current relationship are provided by Equation 1. The detected voltage and injected current relationship have been given by equation 2 [15].

$$V_{\text{out}} = S_{\text{type}} I_{\text{inject}} n_s \cos\left(\frac{2m^* \alpha L}{\hbar^2} + \phi\right) \quad (1)$$

Where, I_{inject} is the injected current, and V_{out} is the voltage received at the output,

$$n_s = \frac{V_{\text{detect}}}{I_{\text{inject}}} = \pm \frac{1}{2} P_j^2 R_N e^{-\frac{L}{\lambda_N}} \quad (2)$$

$$\Delta\theta = \frac{2m^* \alpha L}{\hbar} \quad (3)$$

$$\alpha = k_0 V_G^2 + k_1 V_G + k_2 \quad (4)$$

Where '+' & '-' show the direction of magnetization, R_N = Resistance of Semiconductor Channel, P_j = Intersection Interface polarization current indicates the polarization capacity at intersections. In NFM, L stands for channel length and λ_N for spin-diffusion length, which depends on the channel material's property. Remember that, under the following presumptions, equation 1 gives the Datta-Das theoretical model for detected voltage [19, 27]. A few of these model parameters are fundamental constants, such as the electron's effective mass and reduced Planck's constant, while k_0 , k_1 , and k_2 (fitting constants) are taken from [31] and other experimental results from [32]. Equations 1 and 2 clearly show that the spin polarization decays with the channel length (L).

To accurately simulate and analyse the behaviour of spin-based field-effect transistors (Spin-FETs), a set of well-defined physical and empirical parameters is essential. The effective mass of electrons (m^*), a critical factor influencing carrier mobility and quantum transport, is typically taken as 0.05 times the free electron mass ($m_0 = 9.1 \times 10^{-31}$ kg), reflecting the light effective mass in narrow bandgap semiconductors such as InAs and InSb commonly used in Spin-FET channels [13]. The reduced Planck's constant ($\hbar$), fundamental to quantum mechanical calculations, is employed with a standard value of 1.054×10^{-34} J·s [33]. The junction polarization (P_j), which influences the spin injection efficiency, is assumed to be 50%, consistent with ferromagnet-semiconductor interface properties reported in experimental studies [34, 35]. Channel resistance (R_N) is set to 0.5 k Ω , representing a moderately resistive spin transport path, while the channel length (L) is defined as 800 nm—a practical dimension balancing gate control and ballistic transport [36]. The spin-diffusion length (λ_N), critical for maintaining spin coherence over the channel, is taken as 1 μ m, aligning with values observed in high-mobility spin transport materials [37]. The Spin-FET type (S_{type}) is designated as 1, referring to a specific model or configuration used in the simulation framework. The phase correction factor (ϕ) and empirical fitting coefficients (k_0 , k_1 , and k_2) are included to account for additional spin-orbit interaction effects and to match simulated results with experimental data. In this model, k_0 is set to zero, while k_1 and k_2 are assigned values of -3.4205×10^{-31} and 9.5775×10^{-31} respectively, derived through regression fitting techniques to calibrate the spin precession behaviour in the presence of Rashba spin-orbit coupling [15]. Together, these parameters form the backbone of a robust and scalable Spin-FET simulation model, enabling accurate prediction of spin transport and logic behaviour in spintronic circuits [27]. Figure 2 depicts the QGSFET's construction. Apart from an additional gate terminal, the QGSFET is comparable to the TGSF and DGSF. The output voltage equation for QGSFETs is shown in the equation 5:

$$V_{out} = S_{type} I_{inject} n_s \cos(\Delta\theta_1 + \Delta\theta_2 + \Delta\theta_3 + \Delta\theta_4 + \phi) \quad (5)$$

$$\text{where, } \Delta\theta_1 = \frac{2m^*\alpha_1 L}{\hbar^2}, \Delta\theta_2 = \frac{2m^*\alpha_2 L}{\hbar^2}, \Delta\theta_3 = \frac{2m^*\alpha_3 L}{\hbar^2} \text{ and } \Delta\theta_4 = \frac{2m^*\alpha_4 L}{\hbar^2}.$$

Similarly, the values of α_1 , α_2 , α_3 and α_4 can be acquired by simply substituting V_{G1} , V_{G2} , V_{G3} , and V_{G4} for V_G . The desired logic functionality in the proposed spin-FET devices is achieved by applying appropriate gate voltages, which modulate the channel conductance and thereby control the source-to-drain current. When the gate terminals are sufficiently spaced, the electrostatic influence of one gate on another becomes negligible. This decoupling is primarily attributed to electrostatic screening, a fundamental phenomenon wherein the presence of mobile charge carriers suppresses external electric fields. Screening effectively

limits the spatial extent of electric field penetration, ensuring that adjacent gate potentials do not interfere with each other. This behavior is well-documented in various charge-carrying media such as electrolytes, ionized gases (plasmas), and electronic conductors, including metals and semiconductors [38-40]. In our case, the effect is further enhanced due to the high doping concentration and elevated carrier density in the channel, which result in a significantly reduced Debye screening length, thereby reinforcing the electrostatic isolation between gates.

In most cases, the channel carrier concentration remains intrinsically high due to the use of narrow bandgap semiconductors such as InAs or InSb, which are commonly proposed as channel materials for Spin-FET devices. Consequently, the electrostatic modulation induced by the gate field is significantly screened over a very short spatial extent, owing to the extremely small Debye screening length characteristic of such high-carrier-density materials. This limits the gate's ability to influence the channel potential, thereby posing challenges for effective electrostatic control in spin-based field-effect transistor architectures. Equation 6 provides the formula for determining the Debye screening length.

$$\delta = \sqrt{\frac{\epsilon K T}{e^2 N_a 2C}} \quad (6)$$

Where ϵ = constant of the dielectric, K = Boltzmann's constant, and T = absolute temperature. N_a = acceptor ion concentration of the channel, and C = Avogadro's constant. For an InAs channel with a dielectric constant $\epsilon = 15.15$, a sheet carrier concentration (N_a) of 10^{18} cm $^{-3}$, and a temperature $T = 300$ K, the Debye screening length is roughly 4 nm. We may disregard the interaction between gates if the edge-to-edge spacing between them is greater than 4 nm because it is very challenging to position gates closer than even 10 nm with current technology. This issue has been resolved in the proposed design, which assures that the gate voltages aren't going to interfere.

3. RECONFIGURABLE LOGIC USING QGSFET FOR DIFFERENT OPERANDS

The reconfigurability of the quadruple spin transistor is shown in Figure 4. In the reconfiguration, logic can change the spin-FET behavior after fabrication. External electric fields are applied to manipulate the spin orientation and spin transport. However, magnetic fields are used to control the spin direction. Also, required strong spin-orbit coupling to manipulate spin currents. Major group III-V semiconductors and topological insulators are preferred due to the high mobility of electrons in the region of channels (like GaAs, InAs, and Graphene) [41]. The purpose of a fixed logic gate is predetermined when it is manufactured. The logic function of reconfigurable logic gates is changeable, meaning that it can be altered even after it has been manufactured.

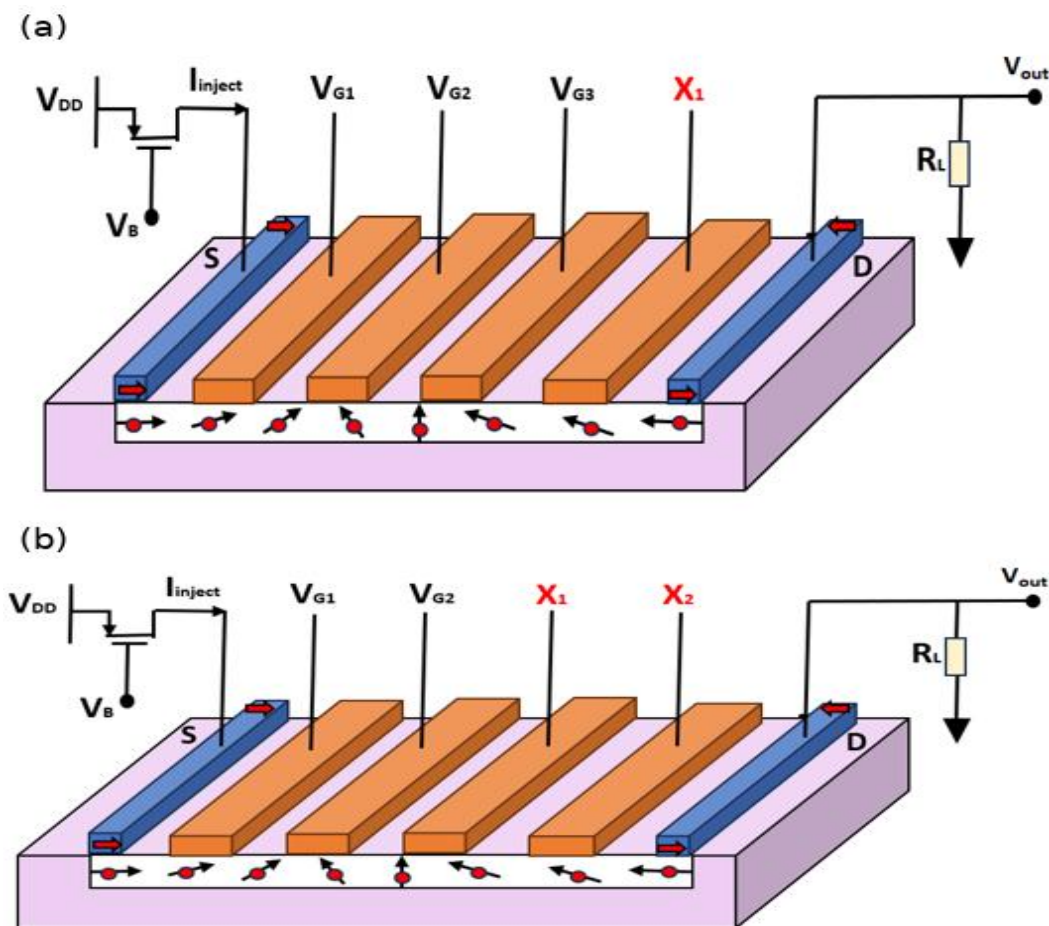


Fig. 4. Reconfigurable QGSFET Structure for (a) 3-operands (b) 2-operands.

In the reconfigurable logic of QGSFET, the four-gate terminal is connected to the 2-DEG channel, where these voltages are used to perform the logical functions at different channel lengths for different operands by setting one gate voltage as the control terminal. This approach provides unique insights into the design and functionality of logic gates that leverage the spin degree of freedom, offering potential advantages in low-power and high-speed applications. Different logic functions are obtained by changing the control voltage of the multi-gate terminal. Only one multi-gate is needed to perform different logic functions after the device has been manufactured, whereas Figure 4 shows the structure for 3-operand and 2-operand QGSFET. The cascading of the multi-gate spin-FETs was used to achieve higher-order logic functions. Also, fixed gate logic gates give particular functions at particular channel lengths on various operands.

An electrically reconfigurable logic gate can change a voltage at one or more control terminals to accomplish several purposes with the same structure. The controlling terminal's function is fixed and unchangeable once the voltage is established. It is essential that spin-based reconfigurable logic offers extra benefits above traditional reconfigurable logic. Most reported works on spin-FET logic

gates focus on basic logic gates (viz., AND, XOR, OR). However, with the help of QGSFET, we can scale to larger combinational circuits. The field of spintronics uses the property of magnetism and has demonstrated success in achieving low power, high speed, and non-volatility due to spin polarization. Its primary use is for look-up tables in an FPGA. Circuit complexity, hardware, and power consumption will all be reduced as a result. It improves the performance of the circuit or gadget. Numerous articles about reconfigurable logic have been published in the open literature. While considering a 2-bit binary adder using QGSFET gives advantages over CMOS, which is explained in the design of 3-operand sections.

3.1. Designing of Three-Operand Functions

In designing three-input logic functions, the fourth gate terminal (V_{G4}) is kept as a control terminal (X), and the first three gate terminals are the inputs (A, B, and C). However, for the DC simulation, the channel length is 800 nm. We set the control voltage X at 0 V and 1 V and varied the V_{G1} from -6 V to 6 V to observe the DC simulation for three input functions. However, for the value at $X = 0$ V, we observe the

XOR (Sum) function, and at $X=1$ V, we observe the XNOR function for the design of Majority gate (MG), i.e., Carry function observed for the 1160 nm channel length when $X=0$ V, and the complement of the MG function was observed at $X=1$ V. Figure 5 shows the DC simulation results of three input functions utilizing QGSFET. It is important to note that for simplicity, the source transistor and bleeder resistor have not been taken into account. Otherwise, the source transistor is used to inject the current into each transistor, and the bleeder resistor is located at each output node. The output's reliance on the channel length is demonstrated by the DC

simulation.

However, the optimal output voltage for logic circuits depends on the length of the channel. The truth table creation of the generated logic function is indicated by the changes in the output peaks and valleys with the input voltages. With the use of two controlling inputs or a single controlling terminal, it may carry out various logical operations. The spin-FET has the intrinsic capacity to reconfigure. Applying a 1.4 V pulse with a 10 ns trans period at the input yields the transient simulation, while parametric analysis yields the DC simulation.

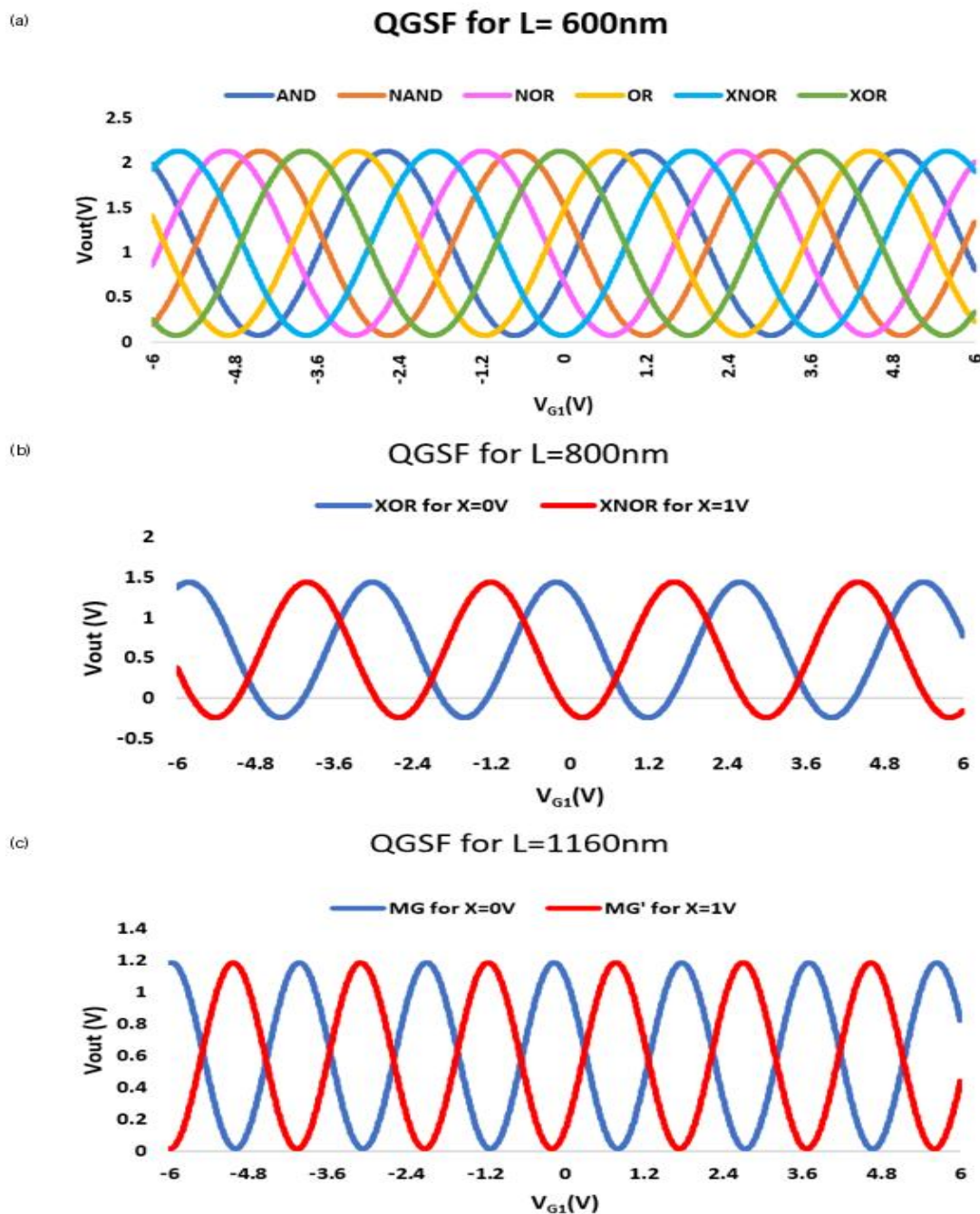


Fig. 5. QGSFET DC analysis for (a) 2-Input operand for $L=600$ nm (b) 3-Input operand for $L=800$ nm (c) 3-Input operand for $L=1160$ nm (d) QGSFET based 1-bit.

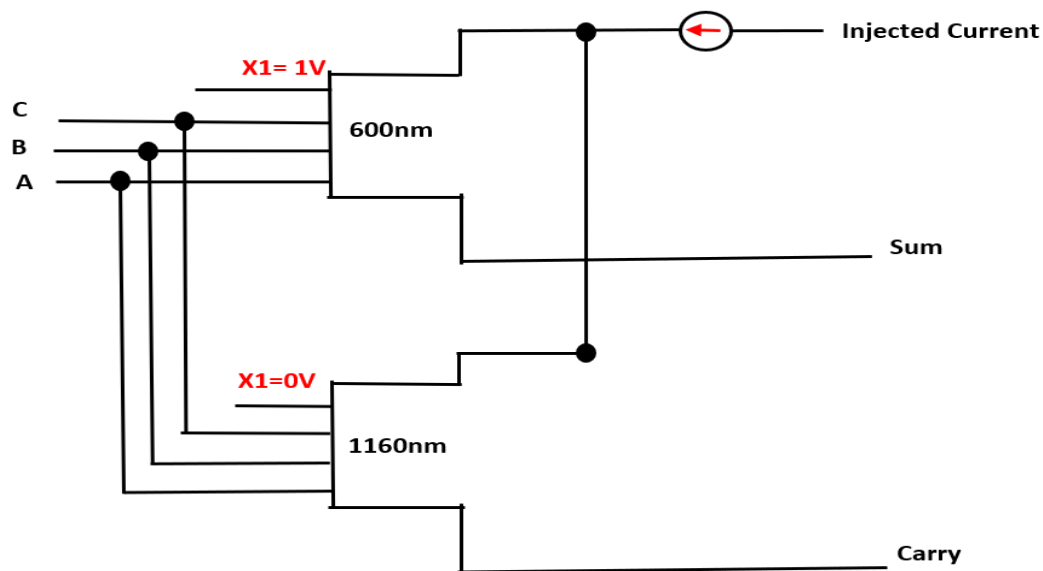

Fig. 6. QGSFET- Based full adder circuit

Table 1. Truth Table of 3-Input function using QGSFE

Inputs			L=800 nm		L=1160 nm	
A	B	C	X=1V $V_{out} (XOR)$	X=0 V $V_{out} (XNOR)$	X=0 V $V_{out} (MG)$	X=1V $V_{out} (MG)'$
0	0	0	0	1	0	1
0	0	1	1	0	0	1
0	1	0	1	0	0	1
0	1	1	0	1	1	0
1	0	0	1	0	0	1
1	0	1	0	1	1	0
1	1	0	0	1	1	0
1	1	1	1	0	1	0

Figure 5 (a) shows the DC simulation results obtained for two inputs by varying the V_{G1} from -6 V to 6 V and keeping V_{G3} and V_{G4} as control terminals to obtain various logic functions where V_{G2} is set to 1.4 V. Figure 5 (b) & (c) shows the DC simulation results for $L=800$ nm & $L=1160$ nm with different control inputs, respectively. Table 1 shows the truth table for three input configurations for three operands. In TGSF, the three logical functions are obtained for different channel lengths [7]. The simulation results were produced by maintaining the first two terminal as a input voltage which fixed at 1.4 V pulse and using the third and fourth gate terminals as control terminals, which vary their voltages from 0 V to 5 V to carry out different logic functions. The output voltages are observed for the different control voltages, and we get several logical functions for two inputs for $L=600$ nm and three inputs for $L=800$ nm. Moreover, we need to set the channel length for the majority gate is $L=1160$ nm, which is

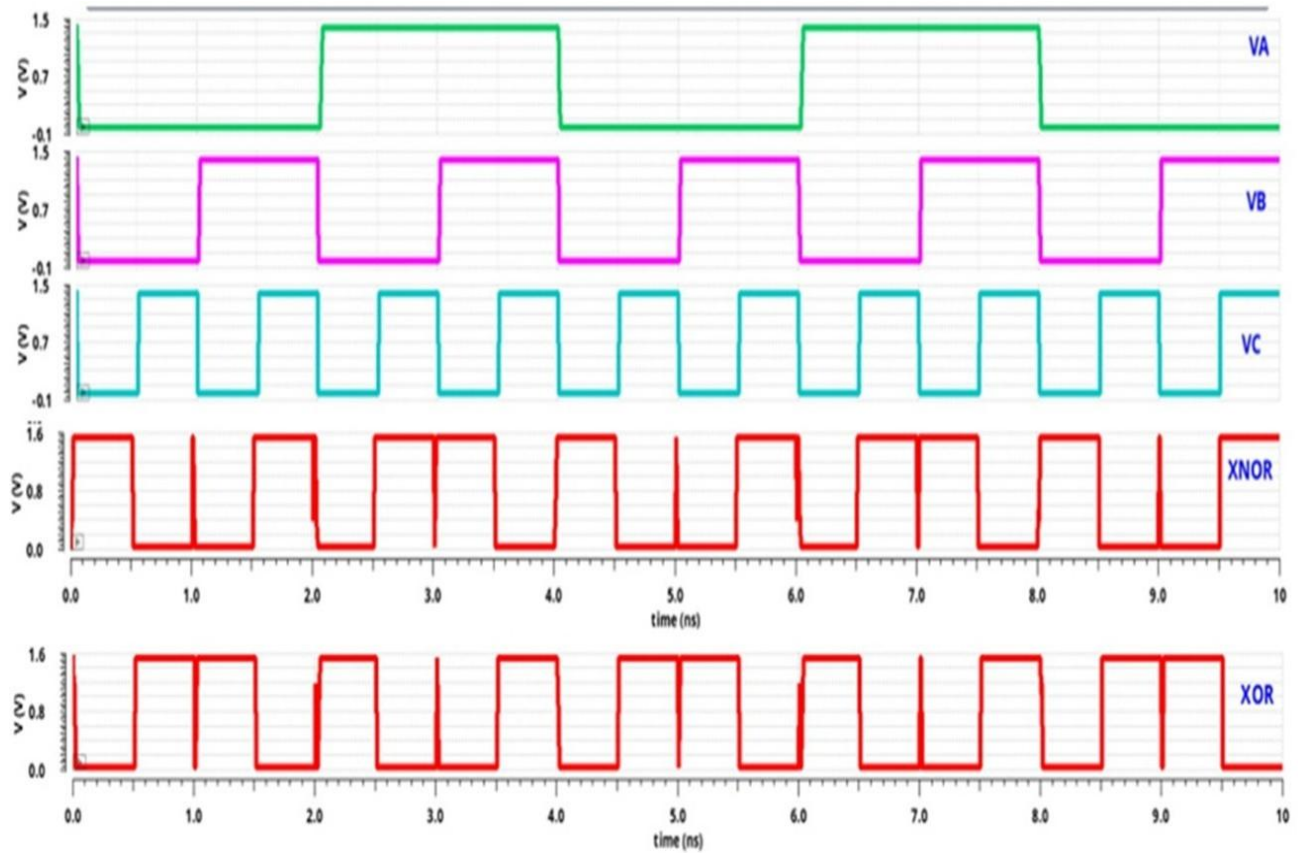
less than TGSF. The control input is set to 0 V to obtain the MG output, and to 1V to obtain the inverse of MG. The design of a 1-bit full adder is also done by using three QGSFETs for the sum and carry output. Figure 6 shows the structure of the QGSFET-based full adder. The output waveform is shown in Figure 7. In QGSFET, we only need two channel lengths to obtain four different logical functions. The transit time and device size are less than existing SFET, which is explained in the performance analysis section. The transient simulation shows the various logical functions using QGSFET.

The results are simulated for a 1 GHz input frequency. However, due to its extremely short response time, the spin-FET is sensitive to the rising and falling edges of the gate voltage. It is important to note that the majority gate's output has several stages. This is because all of the gates use the same signal levels to represent inputs for 1 and 0 signals.

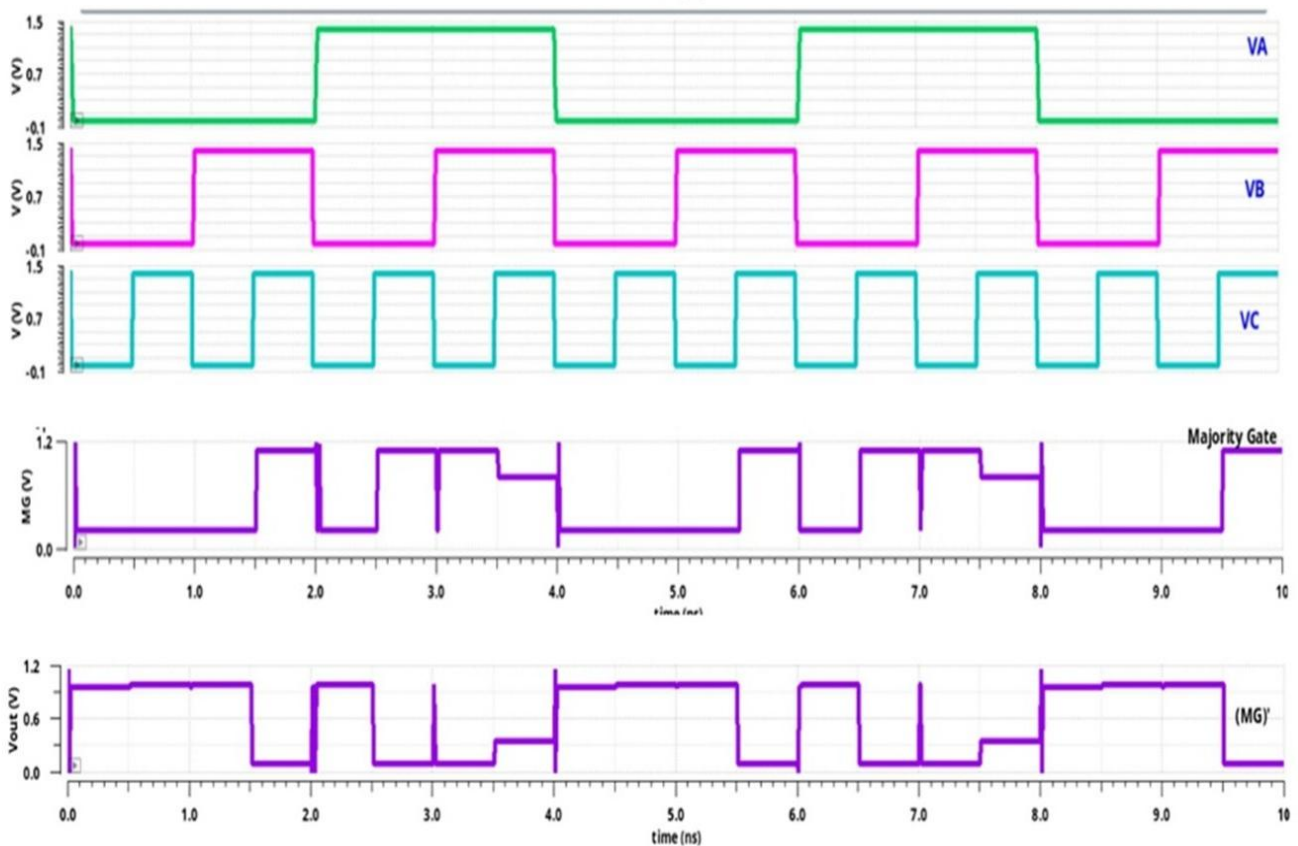
Differentiating the signal levels in the majority gate can help to avoid the issue, but it is not a workable way to provide a consistent logic for the gates. To solve this multi-level issue,

a different approach must be used. A two-bit ripple adder is produced by cascading half and full adders.

(a)



(b)



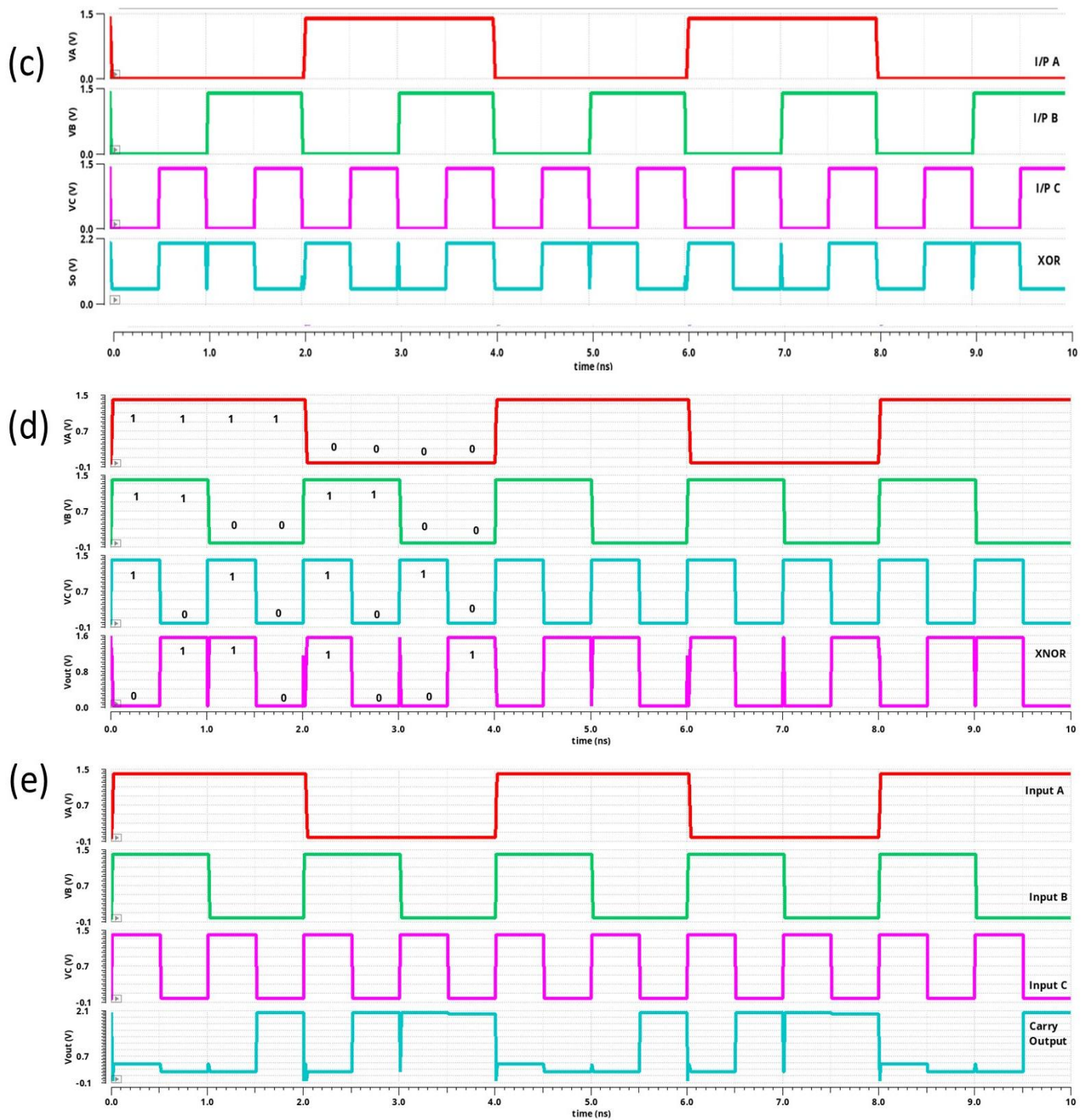


Fig. 7. Transient Simulation of QGSFET for three operands configuration (a) For $L=800\text{nm}$ gives XOR and XNOR logic function for $X=1\text{V}$ and $X=0\text{V}$ respectively (b) For $L=1160\text{ nm}$ gives carry output at $X=0\text{V}$ and $X=1\text{V}$ gives complement operation. Transient simulation for TGSF for three input operands configuration (c) For XOR gate when $L=800\text{ nm}$ (d) For XNOR gate when $L=900\text{ nm}$ (e) For carry output gate when $L=1500\text{nm}$.

The reduction in charge current causes the current to flow through the channel to be pure spin current, and due to that, it is performed under nonlocal geometry, which results in very low output voltages [27, 28, 42, 43]. The output voltage offered at the V_{OUT} stage is very low. The lower drive

capability of spin-FETs involves the clamping and/or amplification of signals before their application to the subsequent stage [7]. Table 2 demonstrates the logic gate truth table for three operands using QGSFET and TGSF. This table summarizes the design parameters, physical dimensions,

and resulting logic functions of a Triple-Gate Spin-FET (TGSF) implementing three-operand digital logic, as reported in foundational multi-gate spintronic literature [7]. The table maps how the physical channel length (L) of a three-gate spin transistor dictates its final Boolean logic behaviour when all three gate terminals are driven by digital input voltages. The QGSFET-based design enables the implementation of multiple logic gates using only two channel lengths by configuring one of the inputs as a control input. This approach facilitates logic gate realization with reduced channel lengths, thereby contributing to device miniaturization and potentially improving circuit integration density. All three gates are consumed by the three input

operands (A , B , C). There is no spare terminal available to modulate or switch the function electrically which shows zero electrically reconfigurability. To switch from an XOR to an XNOR or Majority Gate, the circuit designer must physically alter the channel length during fabrication (800 nm to 900 nm to 1500 nm). Implementing both Sum and Carry in an adder requires laying out devices with mismatched channel lengths, increasing lithographic mask complexity and device footprint. The magnetic or spin-dependent effects that are frequently used in spintronic devices can be sensitive to even small changes in the signal. Figure 7 shows a transient simulation for the three operands for different logic functions using QGSFET.

Table 2. Comparison of 3-operand configurations.

For 3 inputs (V_A , V_B & V_C)		QGSFET		
Channel Length	800nm	1160nm		
Control I/P Voltages (X_1)	1 V	0 V	0 V	1 V
V_{out}	$A \oplus B \oplus C$	$A \odot B \odot C$	$AC + AB + BC$	$(AC + AB + BC)'$
Logical Function	XOR	XNOR	MG	$(MG)'$

For 3 inputs (V_A , V_B & V_C)		TGSF [8]		
Channel Length	800nm	900nm	1500nm	
V_{out}	$A \oplus B \oplus C$	$A \odot B \odot C$	$AC + AB + BC$	
Logical Function	XOR	XNOR	MG	

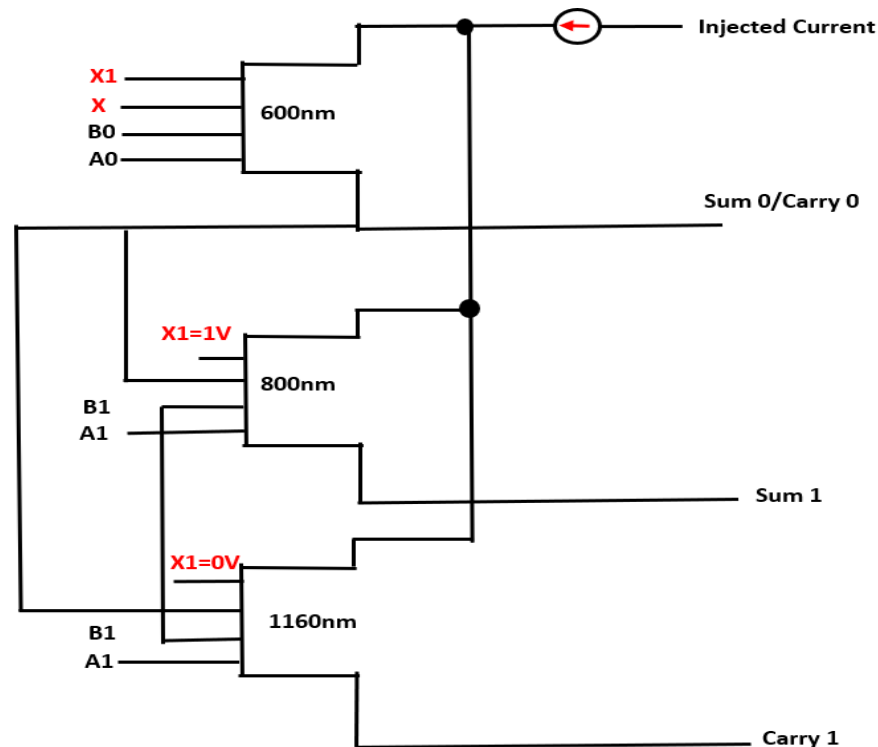


Fig. 8. QGSFET-based 2-bit binary adder circuit.

The functionality of the interfaces and the materials utilized for spin polarization determine how effectively spin injection and detection are performed. Imperfect interfaces and materials with low spin polarization can lead to signal degradation or clamping of the output [44, 45]. The coherence of spin states as they move through the device is constrained by spin relaxation mechanisms (such as electron-phonon interactions, spin-orbit coupling, or hyperfine interaction) [46]. This reduces the strength of the spin signal and prevents it from exceeding a certain threshold. The spin diffusion length sets a maximum distance that spin-polarized carriers can travel before their polarization decays. Beyond this limit, the signal cannot increase further, effectively clamping the output [47].

3.2. Designing of a Two-Bit Binary Adder

The two input bits are A0 A1 and B0 B1, the sum (S0) and

carry bit (C0) are obtained by setting the control voltages of the two operands QGSFET at a 600nm channel length with control voltages X and X1 at 4.5V and 0V for sum output and carry output it sets at 0V and 1.4 V respectively, which shows in Table 5. However, the output of the first QGSFET circuit is connected to the three operands QGSFET by setting the control voltage at 1V at 800 nm channel length to get the final sum output (S1) and for the final carry output (C1) with another QGSFET with control input 0V at 1160 nm. The structure of the 2-bit binary adder using QGSFT is shown in Figure 8, and the transient simulation for the two-bit binary adder is shown in Figure 9.

Only three Quadruple Gate Spin transistors are required to design a two-bit binary adder. Moreover, the number of devices required is less than that of conventional CMOS and the existing spin-FET devices. Using QGSFET reconfigurable logic, we can perform the 2-bit binary operation. The modelling of the 3-input QGSFET has been verified through transient simulation.

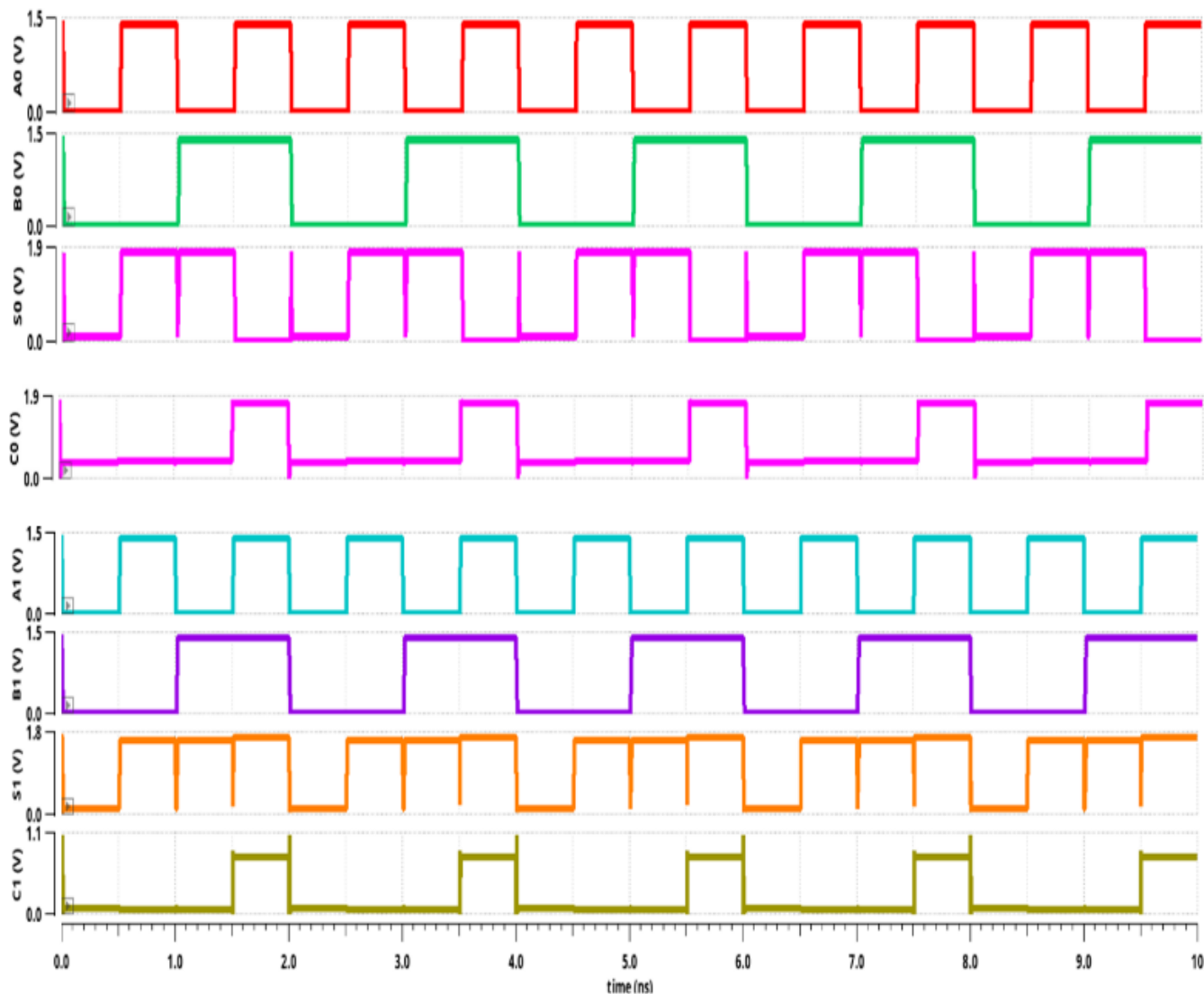


Fig. 9. Transient Simulation of 2-bit binary adder circuit.

Table 3. Comparison of 2-operand configurations with various spin-FETs

For 2-I/Ps (VA, VB)		QGSFET				
L (nm)	600nm					
X	4.5V	1.6V	0V	0V	0V	0V
X1	0V	1V	3.3V	1.4V	1.4V	1.9V
V _{out}	A⊕B	A⊙B	A.B	(A.B)'	A+B	(A+B)'
Logical Function	XOR	XNOR	AND	NAND	OR	NOR

For 2-I/Ps (VA, VB)		TGSF				
L (nm)	900nm		800nm			
X1	1.4V	0V	3.2V	5.1V	3.7V	1.8V
V _{out}	A⊕B	A⊙B	A.B	(A.B)'	A+B	(A+B)'
Logical Function	XOR	XNOR	AND	NAND	OR	NOR

For 2-I/Ps (VA, VB)		DGSF				
L (nm)	723	904	163	325	408	204
V _{out}	A⊕B	A⊙B	A.B	(A.B)'	A+B	(A+B)'
Logical Function	XOR	XNOR	AND	NAND	OR	NOR

3.3. Designing of Two-Operand Functions

The DC analysis of two-operand logic functions using QGSFET is shown in Figure 5. The various logical function operates using only a single channel, Length (L=600 nm) through QGSFET. However, TGSF and DGSF need different channel lengths to perform various logical functions, which affects the device size and requires more transient due to higher channel lengths. Table 3 shows the comparison between the QGSFET, TGSF, and DGSF for the 2-operand function. The various logic function is designed for two inputs using QGSFET by setting different control voltages with single channel lengths. The transient simulation of the 2-input logic function is shown in Figure 10. In prior research (such as Double-Gate Spin-FETs [DGSF] and Triple-Gate Spin-FETs [TGSF]), realizing different Boolean functions required physically modifying the device dimensions during fabrication. In DGSF, implementing these same six basic gates (XOR, XNOR, AND, NAND, OR, NOR) required six completely different physical channel lengths (163 nm, 204 nm, 325 nm, 408 nm, 723 nm, and 904 nm). This geometric dependency made multi-gate spin-FETs unviable for scalable digital manufacturing, as every logic cell needed unique lithographic masks and exhibited mismatched propagation delays [6].

Table 3 demonstrates that by adding two dedicated electrostatic control terminals (X, X1) alongside two data input terminals (VA, VB), all six fundamental Boolean logic gates are implemented within a single, invariant channel

length (L = 600 nm). The circuit designer no longer fabricates different transistors; the logic function is programmed dynamically post-fabrication purely through electrical gate biases [9].

The device operates on the Datta-Das spin precession effect in an InAs 2DEG quantum well channel. The detected drain voltage V_{out} depends cosinusoidally on the total spin precession angle $\Delta\theta_{total}$ where, $V_{out} \propto \cos(\Delta\theta_{total} + \phi)$. Across the four gate segments, the total precession angle is the linear superposition of the phase shifts accumulated beneath each gate.

The modelling of 2-input QGSFET for XOR, XNOR, AND, NAND, OR, and NOR logic functions is verified through transient simulation, which is shown in Figure 10. However, for the generation and detection of parity XNOR function is very useful. While considering the two operands using TGSF, for L=800 nm, it shows logical AND, NAND, OR, and NOR gates, and for L=900 nm, it shows the exclusive gate operation, i.e., XOR and XNOR gates. However, using DGSF for two input variables, we must select different channel lengths to represent each logical function.

Due to variations in the channel length in TGSF and DGSF, the transit time is also higher than that of QGSFET. However, QGSFET has an optimized channel length compared to TGSF and DGSF. The transient simulation of two variables by using QGSFET reconfigurable logic is shown in Figure 10. The performance has been carried out based on the number of devices used to design each logic

function, the speed of the device, and the power consumed by each device based on the capacitances offered by each device to perform a logical function. The performance

analysis of two-input and three-input variables is shown in Table 4.



Fig. 10. Transient simulation for 2-operands QGSFET for different control voltages.

3.4. Transit Time Analysis

The local geometry model's functionality is demonstrated by the transient simulation, which also evaluates the model's performance for circuit applications. The S and D act as injection and detection of electrons, respectively. The simulated results for the logical functions for QGSFET can work for a 1 GHz frequency with a transit time of several picoseconds. The transient time calculation was done using the formula [48], considering the values shown in Table 5.

$$t = \frac{L^2}{2D} + \frac{L}{V_f} \quad (7)$$

Equation 7 provides the delay needed for carriers to traverse the channel. Table 5 displays the default values, which are based on the confirmed studies conducted by H C Koo et al. [25, 28]. The first part of the equation 7, shows the spin diffusive time, and the second term shown in equation 7 is the ballistic time. In modelling the transport properties of Spin-FETs using InAs as the channel material, several fundamental physical parameters play a key role in determining device performance. The electron diffusion coefficient (D) in InAs is typically taken to be $\leq 10^3 \text{ cm}^2 \cdot \text{s}^{-1}$, which reflects the high electron mobility inherent in narrow bandgap III-V semiconductors. This high diffusion constant supports efficient spin and charge transport over relatively long channel lengths, contributing to the feasibility of ballistic or quasi-ballistic operation in nanoscale devices [49]. The channel length (L) is set at 800 nm, a dimension carefully chosen to ensure compatibility with spin-diffusion lengths while also allowing for realistic fabrication under current nano-lithographic capabilities [13]. Another essential parameter is the Fermi velocity (V_f) of electrons in InAs, which is approximated as $C/300$, where C is the speed of light in vacuum ($3 \times 10^8 \text{ m/s}$). This approximation yields a Fermi

velocity on the order of $\sim 10^6 \text{ m/s}$, which aligns with typical values observed in narrow bandgap semiconductors and supports rapid carrier dynamics necessary for high-speed spintronic logic operations [50]. These values collectively underpin the simulation framework for Spin-FETs, enabling accurate modelling of carrier transport and spin dynamics essential for logic gate implementation in spin-based circuits.

However, the obtained delay is about picoseconds for the SFET-based logical function; therefore, it works for the GHz frequency. The high-speed communication system requires a frequency range of several GHz for high-performance of digital circuits. The quantitative simulation majorly depends on the length of the channel and the channel material used in the transistor. The delay time was calculated for InAs channel material. The propagation delay in QGSFET is influenced by capacitance, resistance, and spin lifetime. The transit time for different SFET-based devices is shown in Table 4.

3.5. Power Analysis of Spin-FET

The power delay product (PDP) calculation for a QGSFET involves analysing both power dissipation and propagation delay, the key metric in nano-electronic and spintronics devices. The PDP metric is used for low-power devices and is the product of total power and spin lifetime, which can be optimized by reducing V_{DD} , increasing spin lifetime, and reducing junction capacitances and resistance [51]. The prior studies often focus only on dynamic power however, with the help of QGSFT, we can also reduce static power consumption using high spin-polarized materials (viz. Heusler alloys), high- k dielectrics for avoiding gate leakage, increasing spin lifetime by using materials with high spin-orbit coupling, and optimized ferromagnetic layer thickness [52, 53].

Table 4. Transit Time for Logic Function for 3-operands and 2-operand configurations.

For 3-operands	QGSFET			TGSF	
Channel Length (L)	800nm	1160nm	800nm	900nm	1500nm
Logic Function	XORXNOR	MG(MG)'	XNOR	XOR	MG
t	0.8ps	1ps	0.8ps	0.9ps	1.5p

For 3-operands	QGSFET	TGSF				DGSF			
Channel Length (L) nm	600	900	800	723	204	163	904	325	408
Logical Function	XOR, OR, NOR XNOR AND, NAND	XNOR, XOR, OR	AND, NAND	XOR	NOR	AND	XNOR	NAND	OR
t	0.6ps	0.9ps	0.8ps	0.7ps	0.2ps	1.5ps	0.9ps	0.32 ps	0.4ps

$P = C f V_{DD}^2$ is the estimated dynamic power consumption of the logic gates. V_{DD} stands for the bias voltage, f for the input frequency, and C for the capacitance. The power dissipation for the circuits using the proposed QGSFET design, where the capacitance $C = 4C_{GATE} + C_{LOAD}$, the capacitance $C = 3C_{GATE} + C_{LOAD}$, and $C = 2C_{GATE} + C_{LOAD}$ [27, 28], will be nine microwatts for the TGSF, ten microwatts for the QGSFET, and eight microwatts for the DGSF, assuming that C_{GATE} and C_{LOAD} are equal to 1 fF and 6 fF, where V_{DD} is 1V at a frequency of 1GHz.

The proposed quadruple-gate spin-FET (QGSFET) exhibits an energy dissipation as low as 10 femtojoules per operation, highlighting its potential for ultra-low-power logic applications. When multiple QGSFET devices are cascaded, the total energy dissipation is the cumulative sum of individual device energies, as demonstrated in [24]. In contrast, previously reported studies have not thoroughly analysed energy efficiency, particularly in the context of multi-gate spin-FET architectures. The QGSFET achieves minimal energy consumption per logic operation, owing to its optimized design and efficient charge-spin transport mechanism. Furthermore, the device exhibits shorter transit times and requires fewer components to implement complex logic functions compared to traditional CMOS circuits and earlier spin-based logic implementations, as summarized in Table 5. This reduction in device count, power consumption, and propagation delay translates to significant improvements in overall circuit performance. When comparing the performance of various logic families, the advantages of spintronic architectures become increasingly evident. As we progress from conventional CMOS to dual-gate (DGSF),

triple-gate (TGSF), and ultimately quadruple-gate (QGSFET) spin-FET configurations, a clear trend of enhanced efficiency, compactness, and functional scalability emerges, establishing QGSFET as a promising candidate for next-generation, energy-efficient reconfigurable logic systems.

CMOS logic circuits typically require a higher device count, which results in increased circuit area and power consumption. In contrast, spin-FET-based devices, particularly QGSFETs, achieve logic functionality with the lowest device count due to their intrinsic capability to implement multi-input logic within a single device structure [54]. Power dissipation is another critical parameter where spin-based architectures show superiority. While CMOS exhibits high dynamic and leakage power, QGSFETs benefit from charge-less spin current transport, resulting in minimal energy dissipation [34]. Performance-wise, CMOS technology generally operates in the ~1–2 GHz range, whereas spin-FET architectures demonstrate significantly higher operational speeds, with QGSFETs capable of exceeding 8 GHz due to faster spin dynamics and lower parasitic delays [55]. Furthermore, reconfigurability is inherently absent in CMOS-based logic, requiring substantial hardware redesign to change logic functionality. Spin-FETs, especially QGSFETs, support full reconfigurability, enabling both 2-input and 3-input logic operations dynamically via gate voltage control [21]. This combination of low device count, ultra-low power, high-speed operation, and full logic reconfigurability positions QGSFETs as a promising candidate for next-generation, energy-efficient logic circuits. Table VI shows the different metrics for CMOS and existing Spin-FETs

Table 5. Performance Analysis of 3-operands and 2-operand configurations.

Devices Required	CMOS	DGSF [6]	TGSF [7]	QGSFET (Proposed)
2-Input AND & OR Gate	6	1	1	1
2-Input NAND & NOR Gate	4	1	1	1
2-Input XNOR & XOR Gate	10	1	1	1
3-Variables XNOR & XOR Gate	12	3	1	1
Majority Gate	10	3	1	1
Full Adder	28	5	2	2
2-bit Binary Adder	56	10	4	3

Table 6. Different Metric for CMOS and Spin-FET Devices.

Metric	CMOS	DGSF	TGSF	QGSFET
Device Count	High	Medium	Low	Lowest
Power Dissipation	High	Moderate	Low	Lowest
Speed (GHz)	~1-2	~5	~8	<10
Reconfigurability	No	Partial	Partial	Full (2 & 3 -input Logic)

Table 7. Fabrication Challenges and Their Causes, Impacts, and Possible Solutions.

Challenge	Cause	Impact	Possible Solution
Multi-terminal fabrication	Complex lithography and etching	Misalignment, resistance imbalance	EBL, self-aligned gates, precision lithography
Spin injection inefficiency	Conductivity mismatch	Low polarization, weak signal	Tunnel barriers, optimized FM materials
Spin relaxation and decoherence	SOC, hyperfine interactions	Reduced coherence length	Low-SOC materials, surface passivation
Spin precession control	Gate voltage variability	Inconsistent logic states	Independent gate control, multi-gate calibration
Magnetic anisotropy variation	Strain-induced effects	Misaligned spins	Strain-engineered FM layers
Channel synchronization	Transport time variations	Phase mismatches	Calibrated channel lengths, synchronization circuits
Low signal-to-noise ratio	Noise accumulation	Reduced readout accuracy	LNAs, shielding, noise-reduction techniques
CMOS integration challenges	Fabrication incompatibility with CMOS	Complex integration, scaling issues	Hybrid spin-CMOS platforms

In the case of QGSFET, the transit time is less than the other two devices shown in Table 6. While considering the dynamic power consumption in the QGSFET is 50% to 60% less as compared to that of CMOS. However, to implement 2-operand logic gates, we design all logical functions with a single channel length compared to the reported devices. Moreover, for three operands, we need only two channel lengths for the implementation of four logical functions using QGSFET. However, single-channel lengths perform single logical functions using TGSF and DGSF.

4. POTENTIAL FABRICATION CHALLENGES IN QUADRUPLE SPIN-FET

The intricate nature of spin transport, spin injection, and spin manipulation makes fabricating spin field-effect transistors (Spin-FETs) challenging from a technical and material standpoint [17]. Four spin-polarized channels or terminals make up the Quadruple Spin-FET (QSFET), a more sophisticated version of the ordinary Spin-FET that allows for greater signal processing and multi-state logic operations [37]. However, because of their greater complexity, sensitivity to spin interactions, and more stringent material requirements, constructing such devices presents extra hurdles. Table 7 shows significant fabrication challenges associated with QSFETs [56, 57].

Research is concentrated on 2D materials (like graphene) with longer spin lifetimes in order to get around these fabrication issues [58]. Enhance spin injection methods with more effective interfaces. Interconversion layers with spin-

charge for improved CMOS compatibility. Hybrid, scalable spin-CMOS designs for real-world uses. The realization of reliable, effective, and scalable Spin-FETs for the next spintronic logic and memory devices depends on these developments [56, 59]. The QSFETs involve multi-layer fabrication, making CMOS-compatible integration challenging. To overcome this, we can use the hybrid spin-CMOS platforms and advanced lithography techniques. Also, to maintain the spin coherence, the Heusler alloys or topological insulators are used at room temperature [57].

Integrating Quadruple Spin-FETs (QSFETs) with current CMOS fabrication has the potential to transform spintronics into a practical and scalable technology. Real-world implementations will benefit to Low-power, high-speed computing with multi-state logic operations, and energy-efficient memory with QSFET-based MRAM. Spin-logic processors with superior performance. As fabrication techniques improve, QSFETs will become more viable for commercial spintronic applications, boosting their impact on next-gen computing and memory technologies [54].

5. CONCLUSION

In this work, we propose the modelling and simulation of a quadruple-gate spin-FET (QGSFET) architecture by modifying the channel length to support a wide range of logic operations for both 2-input and 3-input operands. The concept of reconfigurability is central to this approach, enabling the realization of various logic functions through the application of control voltages to the gate terminals. The

flexibility of the QGSFET architecture allows for the dynamic configuration of logic functions without requiring structural modifications. We have further demonstrated the practical application of QGSFETs by designing adder circuits, validating their logical correctness through detailed DC analysis. This analysis also examines the influence of channel length on logic performance, particularly in terms of functional reliability and output characteristics. The proposed QGSFET-based solutions offer a more compact footprint and significantly lower power consumption compared to conventional CMOS logic gates and previously reported spin-based devices. In comparison to dual-gate (DGSF) and triple-gate (TGSF) spin-FET configurations, QGSFETs exhibit enhanced performance, achieving multiple logic operations with a single optimized channel length and reduced carrier transit time. The multi-gate configuration enables the development of novel, energy-efficient, and reconfigurable logic circuits, suitable for next-generation low-power systems.

This study primarily emphasizes minimizing power consumption, propagation delay, device count, and energy dissipation per logic operation, while maximizing functional reconfigurability. Additionally, it discusses potential fabrication challenges associated with the QGSFET structure and its implications on device performance, as well as proposes feasible solutions to address these challenges.

DECLARATIONS

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Conflict of Interest

The authors declare that they have no conflict of interest regarding the publication of this paper.

Data Availability Statement

All data supporting this study's findings are included within the article. The data supporting this study's findings are available upon reasonable request from the authors.

Compliance with ethical standards

This article does not contain any studies with human or animal subjects.

Clinical trial

Not applicable

Clinical Ethics

Not applicable

Consent to Participate

Not applicable

Consent to Publish

Not applicable

Authors' contributions

All authors contributed to the design and simulation. Material preparation, data collection, and analysis were performed by Priti J. Rajput, Dr. Sheetal U. Bhandari, and Salman Firdous. The first draft of the manuscript was written by Priti J. Rajput, and Salman Firdous. All authors read and approved the final manuscript.

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